Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, Tokyo, 2001, pp. 106–107

D-2-5

Origin of Critical Substrate Bias in Variable Threshold Voltage CMOS

Takashi Inukai [1], Hyunsik Im [1] and Toshiro Hiramoto [1,2]

[1] Institute of Industrial Science, University of Tokyo, 4-6-1 Komaba, Meguro-ku, Tokyo 153-8505, Japan
Phone:+81-3-5452-6264 Fax:+81-3-5452-6265 E-mail: inukai@nano.iis.u-tokyo.ac.jp
[2] VLSI Design and Education Center, University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8656, Japan

1. Introduction

Variable threshold voltage CMOS (VTCMOS) has recently attracted much attention for ultra-low power LSI applications at low supply voltage (V_{dd}) [1-4]. Utilizing the body effect, the threshold voltage (V_{th}) can be controlled by the substrate bias (V_{bs}), which makes it possible to obtain high V_{th} in the stand-by mode and low V_{th} in the active mode in the same devices. Therefore, while *off*-current in the stand-by mode is fixed to low level, *on*-current can be enhanced in the active mode. The V_{th} shift is given by

$$\Delta V_{th} = \gamma |\Delta V_{bs}|, \qquad (1)$$

where γ is the body effect factor [5]. According to eq.(1), larger γ results in larger ΔV_{th}, but it is well known that the devices with larger γ have smaller *on*-current due to degraded subthreshold characteristic and smaller transconductance [5]. Koura et al. have systematically investigated these competing factors and found that larger γ results in higher *on*-current when the substrate bias can be changed more than a critical voltage (V_o) [6], as shown in Fig. 1. Therefore, V_o is a very important parameter in VTCMOS, because the optimum design of γ depends on relation between $|\Delta V_{bs}|$ and V_o. Smaller V_o is desirable to obtain higher *on*-current. However, the mechanism that determines V_o has not been fully understood. In this paper, we have studied the origin of V_o by means of device simulation [7] and found that V_o has two different components. It is also found that V_o is scaled as the technology advances and VTCMOS will be very effective in the future.

2. Simulation and Results

Figure 2 shows the device structure assumed in this work. Assuming an ideal step-shape profile and changing depth and concentration of the upper layer, the depletion width (hence γ) and V_{th} can be independently changed. Figure 3(a) shows the dependence of active *on*-current on $|\Delta V_{bs}|$ and γ at a fixed $I_{off,standby}$. It is found that there is a critical value of $|\Delta V_{bs}|$ (V_o) and larger γ results in higher *on*-current when $|\Delta V_{bs}| > V_o$. On the other hand, Fig. 3(b) shows the dependence of the threshold voltage on $|\Delta V_{bs}|$ and γ. It should be noted that another critical value of $|\Delta V_{bs}|$ (V_{o1}) can be defined in terms of V_{th}. When $|\Delta V_{bs}| < V_{o1}$, larger γ results in higher V_{th} in the active mode, while larger γ results in lower V_{th} when $|\Delta V_{bs}| > V_{o1}$.

3. Discussions

Two Components of V_o

Since there are two drawbacks to the devices with larger γ, V_o is expected to have two components. One is a voltage to compensate for the degraded subthreshold characteristics and the other for the degraded transconductance. Figure 4 illustrates the compensation mechanism. Without the substrate bias ($|\Delta V_{bs}| = 0$V), *on*-current of larger γ device is smaller due to not only higher V_{th} but also smaller transconductance. When $|\Delta V_{bs}| = V_{o1}$, the difference of V_{th} due to degraded subthreshold characteristics is cancelled, while *on*-current remains lower due to smaller transconductance. Therefore, in order to achieve the same *on*-current, further substrate bias ($=V_{o2}$) is required. V_{o2} is considered to compensate for the degraded transconductance and defined as the difference between V_o and V_{o1} (i.e. $V_o = V_{o1} + V_{o2}$).

Dependence of V_o on $I_{off,standby}$ and V_{dd}

V_{dd} decreases as technology advances and $I_{off,standby}$ changes depending on the applications. Therefore, dependence of V_o on them is one of the concerns. Figure 5(a) shows the $I_{off,standby}$ dependence of V_o. It is interesting to notice that V_{o1} and V_{o2} have the opposite dependency. As $I_{off,standby}$ increases, V_{o1} decreases due to decreasing difference of V_{th} with the same *off*-current [8]. On the other hand, as $I_{off,standby}$ increases, V_{o2} increases. This is due to the increase of gate overdrive (V_{dd}-V_{th}), which makes *on*-current less sensitive to V_{th} and requires larger ΔV_{th}. This dependence of V_{o2} on gate overdrive can be seen more clearly in the V_{dd} dependence. Figure 5(b) shows the V_{dd} dependence of V_o. While V_{o1} has no dependence on V_{dd}, V_{o2} drastically decreases with decreasing V_{dd}, which results in the reduction of V_o.

Trend of V_o in the Future

Figure 6 shows the trend of V_o and its components. Two scaling scenarios are assumed for the stand-by *off*-current according to ITRS [9]. As technology advances, both V_{o1} and V_{o2} decrease due to the increase of $I_{off,standby}$ and the reduction of V_{dd}, respectively. These results indicate that the required $|\Delta V_{bs}|$ for high *on*-current will be scaled down and VTCMOS can maintain its advantage in the future.

4. Conclusions

The critical substrate bias, V_o, which is one of the most important parameters in the optimum design of VTCMOS, has been systematically investigated and clarified. It is found that V_o is determined by two mechanisms, which have been successfully separated and evaluated. One is related to subthreshold characteristics and depends on *off*-current, while the other is related to transconductance and depends on supply voltage and *off*-current. It is also found that V_o will decrease in the future and hence the devices with large γ will keep its effectiveness in VTCMOS.

Acknowledgement

The authors would like to thank Prof. T.Sakurai for fruitful discussions. This work was partly supported by JSPS Research for the Future Program and by the Grant-in-Aid for Scientific Research from the Ministry of Education, Culture, Sports, Science and Technology. The device simulator (Medici™) has been supplied through VLSI Design and Education Center (VDEC), the University of Tokyo with the collaboration by Avant! Corporation.

References

[1] T. Kuroda et al. IEEE J.Solid-State Circuits, **31** (1996) 1770.
[2] Y. Oowaki et al. ISSCC Tech. Dig. (1998) 88.
[3] H. Mizuno et al. ISSCC Tech. Dig. (1999) 280.
[4] T. Hiramoto et al. Extended Abstract of SSDM (2000) 372.
[5] T. Hiramoto et al. IEICE Trans. Electronics, **E38-C** (2000) 161.
[6] H. Koura et al. Jpn.J.Appl.Phys. **39** (2000) 2312.
[7] Medici Ver.4.1, Avant! Corp., July 1998.
[8] H. Im et al. ISLPED Tech. Dig. (2001) [in press].
[9] International Technology Roadmap for Semiconductors, 1999 Version.

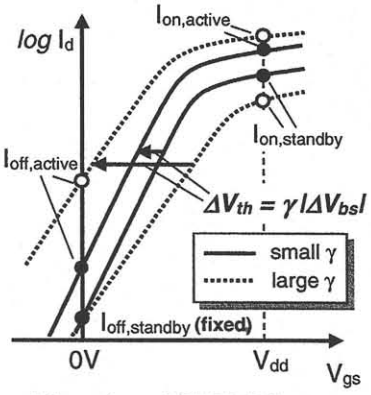

Fig. 1 Schematics of VTCMOS characteristics with different γ. Degraded *on*-current of large γ devices can be compensated and higher *on*-current can be achieved by utilizing VTCMOS when $|\Delta V_{bs}|$ is larger than a critical value (V_o).

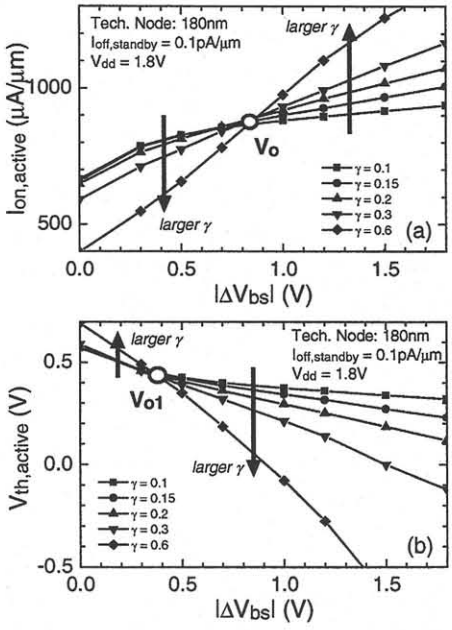

Fig. 3 Dependence of characteristics in the active mode on $|\Delta V_{bs}|$ and γ. (a) *On*-current and (b) V_{th}. There are two critical values of $|\Delta V_{bs}|$, V_o and V_{o1}, in terms of *on*-current and V_{th}, respectively.

Table 1 Device parameters for simulations.

Tech. Node	180nm	130nm	100nm	70nm	50nm	35nm
L_g (nm)	140	85	65	45	32	22
V_{dd} (V)	1.8	1.5	1.2	0.9	0.6	0.4
T_{ox} (nm)	3	2.5	2	1.5	1	0.7
X_j (nm)	50	35	30	20	15	10
I_{off} (nA/μm) [High Performance]	5	10	20	40	80	160
I_{off} (pA/μm) [Low Power]	5	10	20	40	80	160

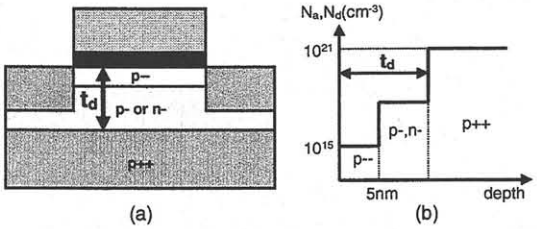

Fig. 2 A device structure assumed in the device simulations. (a) A schematic of the structure and (b) the profile of channel. Assuming an ideal step shape, the depletion width is controlled by the depth of the second layer and V_{th} is controlled by the concentration and type of dopant. A non-doped layer with 5nm thick (N_a = $10^{15}cm^{-3}$) is inserted in order to avoid the inaccuracy of model for the dependence of mobility on the impurity concentrations.

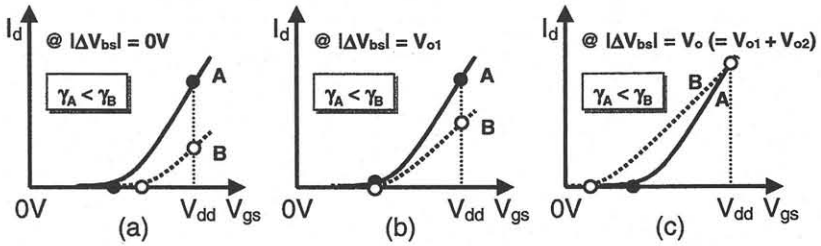

Fig. 4 Schematics of compensation mechanism for the degraded *on*-current in the device with large γ by VTCMOS. (a) When $|\Delta V_{bs}|$ = 0V, larger γ device has smaller *on*-current due to higher V_{th} and smaller g_m. (b) When $|\Delta V_{bs}| = V_{o1}$, V_{th} becomes same as that of smaller γ device, while the *on*-current remains smaller due to smaller g_m. (c) When $|\Delta V_{bs}| = V_o$, smaller g_m is compensated by lower V_{th} and the same *on*-current is achieved as smaller γ device.

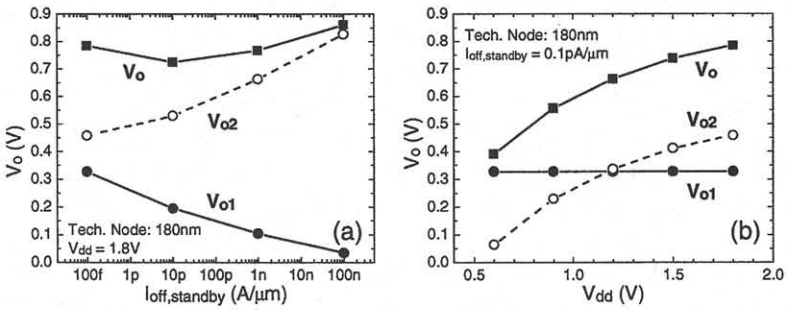

Fig.5 Dependence of V_o and its components on (a) $I_{off,standby}$ and (b) V_{dd}. V_{o2} is derived from V_o and V_{o1}.

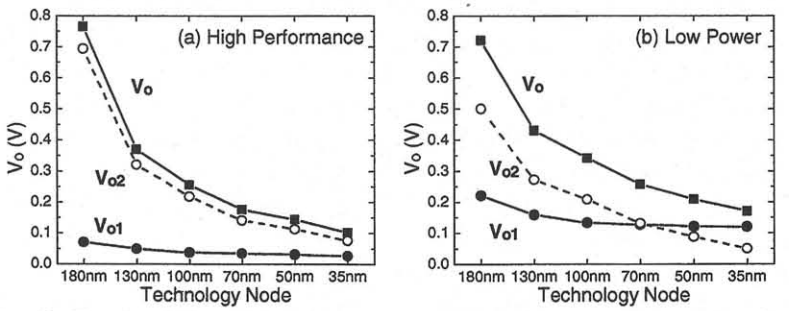

Fig. 6 Trends of V_o and its components. The device parameters are based on ITRS (Table 1) [9]. Two scenarios for stand-by *off*-current are assumed. (a) High performance and (b) low power.