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A New Photodiode Structure with Spacer Window for High Sensitivity 0.35-μm CMOS Imagers

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1. Introduction

CMOS image sensors have the advantages of low voltage supply, low power consumption, random access of the image data, and compatibility with standard CMOS logic technology, [1,2]. CMOS imagers fabricated by 0.5μm or above CMOS technology was able to provide acceptable performance due to the less stringent process requirement in contact, isolation and junction formation, [3]. As the CMOS technology is scaled to 0.35μm or less; the standard CMOS logic process with shallow source/drain junction and silicidation drastically degrades the performance of photo-sensing cells. The optically opaque silicide layer above the n+ diffusion region presents the most serious problem of preventing light penetration, [4]. Furthermore, the silicided shallow junction is reported to have higher leakage current, [5]. Process of forming nonsilicided source/drain pixel is available by using organic material spin coat and etches back, [6]. The process however is not completely compatible to standard CMOS logic technology and required additional mask in fabrication.

In this work, we propose a new photodiode structure with spacer windows, which can improve the sensitivity of CMOS imagers fabricated by or beyond 0.35μm CMOS standard logic technology. Comprehensive study of the design of novel structure is presented as well.

2. Novel Photodiode structure and Layout

The spectral sensitivity of the p-n junction photodiode fabricated by 0.35μm CMOS logic process is expected to reduce significantly due to the optically opaque silicide layer on top. To increase light penetration to the photo-sensing junction, optical windows formed by spacers are designed, as shown in Fig.1. The layout of the novel sensor pixel is shown in Fig.2. The n+ poly-silicon finger and the gate poly-silicon for transistors are deposited at the same time. Subsequently, no silicide layer is formed on the silicon-dioxide spacer between the fingers (as shown in Fig.1). To investigate the relationship between pixel sensitivity and spacer window area, cells with various poly-silicon ranging spacing to poly-silicon from 0.2μm to 0.6μm is studied. The width of the poly-silicon finger is 0.5μm.

3. Sample Fabrication and Measurement Condition

The photodiode sensor with pixel dimensions of 7.5μm x 7.5μm was fabricated by TSMC silicided 0.35μm CMOS logic process. The architecture of our sensor pixel illustrated in Fig.3 contains a photodiode, a reset transistor M_1, an in pixel source follower M_2, and a select transistor M_3. Through giving the reset pulse from pulse generator, the voltage drop of node V_{out} during the integration time is measured. Fig.4 shows the measured waveform from the oscilloscope. The reset signal is a 1ms of 3V pulse with period of 10ms. Six different illumination levels are used to extract the spectral sensitivity. As shown in Fig.4, the slope of the output voltage drop increases with increased illumination intensity. The conventional method of correlated double sampling (CDS) is directly applied to extract the output signal. The relationship between pixel output voltage drop and illumination intensity is illustrated in Fig.5. The pixel spectral sensitivity with the unit V/lux-sec is then obtained by fitting slope of the line in Fig.5. Also, the dark signal level is measured in a similar way, with zero illumination intensity and 500ms integration time to amplify the signal.

4. Experimental Results & Discussions

For comparison, the conventional photodiode formed by simple N+/P junction and the novel diode structure with spacer windows along poly finger structure are fabricated by the same process. Fig.6 shows the cumulative probability of the pixel sensitivities. And the cumulative probability of pixel dark signal is shown in Fig.7. It is found that the pixel sensitivity is 60% higher for the cell with the oxide spacer windows. Since the junction edge increases, the dark current level is expected to increase. However, the dark signal level is found to be similar to that of the conventional photodiode, which means the poly-finger does not induce extra leakage current. Fig.8 shows the relationship between pixel spectral sensitivity and the area percentage of the spacer windows to the original photo-sensing region. Apparently, higher pixel sensitivity can be obtained by further optimization of the spacer window area. The performance comparison of the novel cell and conventional cell are summarized in Table I.

In addition, different bias voltage on poly-finger will result in different sensitivity, shown in Fig.5. Pixel sensitivity decrease when poly-finger bias increases. Special feedback circuit can be designed to apply bias and modify sensitivity depending on illumination. This method allows for improve dynamic range without reducing sensitivity at low intensity levels. For example, the diode output can be connected to V_{poly} through a inverter feedback circuit as shown in Fig.9. By designing suitable transfer for the inverter (eg. 1.4V), a more desirable sensitivity curve can be obtain, (see Fig.10). Sensitivity can be modified at different illumination levels, thus the output signals can be modified at saturate at higher extended intensity levels.

5. Conclusions

A new photodiode structure with oxide spacer window is proposed in this work. The experimental results demonstrate that the new proposed cell fabricated by 0.35 standard logic process can provide sensitivity increase of as high as 60% without any modification in the processing steps and conditions. Optimization of the window area can further improve the imaging sensitivity of CMOS active pixel sensors. By applying bias on the poly finger, sensitivity can be modified at higher illumination to improve dynamic range.

References
[1] E. Fossum, Proc. SPIE, vol.1900, p.2-14, 1993
[2] B. Ackland, et al, ISSCC Dig. , p.22-25, 1996
[3] A. J. Blanksby, et al, IEEE Tran. on ED, p. 55-64, 2000
[4] H. S. Wong, IEEE Tran. on ED, p.2131-2142, 1996
[5] H. D. Lee, et al, IEEE Tran. on ED vol.45 p.1848-1850, 1998
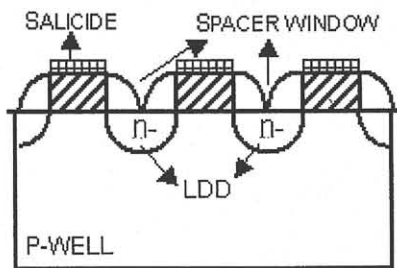[6] D. N. Yang, et al, IEEE EDL, p. 71-73, 2001

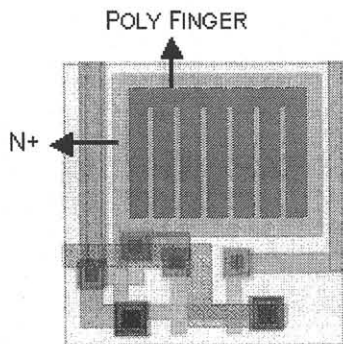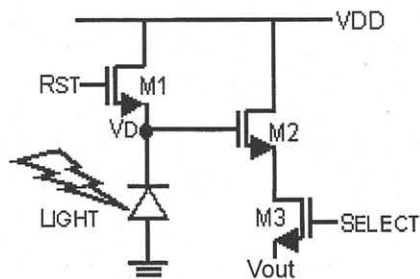Fig. 1 Phtodiode with optical window formed by oxide spacers

Table I. Pixel Performance Comparison

Pixel Type		Original	Poly-Finger
Design	Technology	0.35um CMOS with salicide	
	Pixel Size	7.5um X 7.5um	
	Operation Voltage	3.3V	
	Fill Factor	34%	34%
Experi-mental	Saturation Signal (V)	1.6	1.6
	Dynamic Range (dB)	64	62
	Sensitivity (V / lux*sec)	1. 67	2. 76
	Dark Signal (mV / sec)	~125	~125

Fig. 2 Layout for poly finger structure

Fig. 3 Pixel Architecture

Fig.4 Waveform of reset voltage and output voltage with V_{dd}=3.3V V_{reset}=3V.

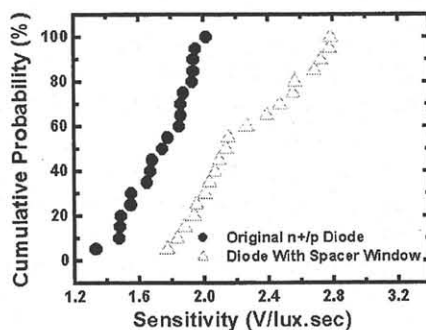Fig. 5 Pixel output voltage drop versus illumination intensity.

Fig. 6 Cumulative probability of pixel sensitivity for different diode structure.
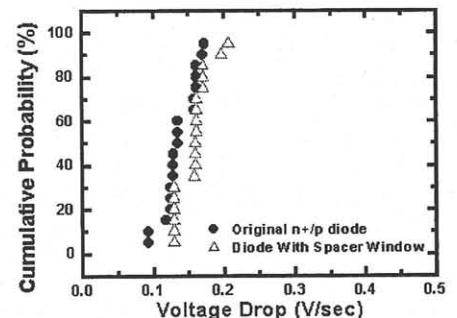

Fig. 7 Cumulative probability of pixel dark signal for different diode structure.
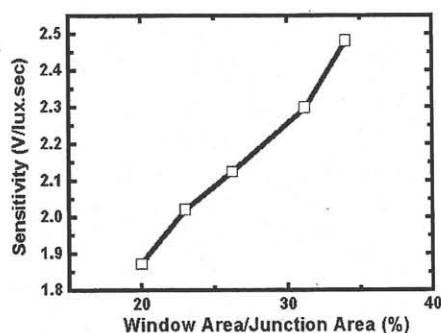

Fig.8 Dependence of sensitivity on the area percentage of spacer window to junction area.
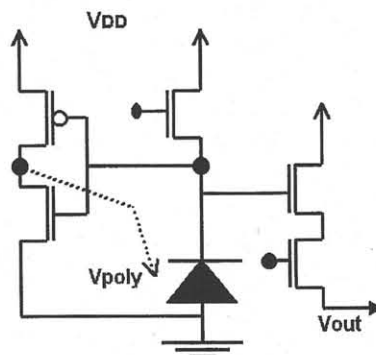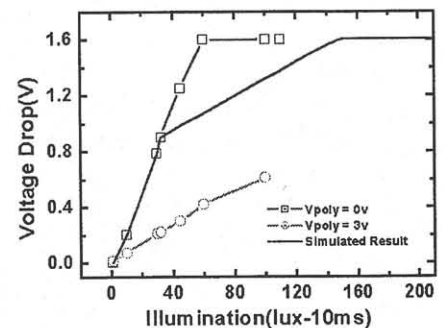

Fig.9 APS with feedback circuit.

Fig.10 Dynamic range improvement simulation result.