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# Characterization of Tunnel-Barriers in Polycrystalline Si Point-Contact Single-Electron Transistors

Y. Furuta[1,4*], H. Mizuta[1,4], K. Nakazato[1,4], T. Kamiya[2,4], Y. T. Tan[2,4], Z. A. K. Durrani[2,4] and K. Taniguchi[3]

[1]Hitachi Cambridge Laboratory, Hitachi Europe Ltd., Madingley Road, Cambridge, CB3 0HE, UK
[2]Microelectronics Research Centre, University of Cambridge, Madingley Road, Cambridge CB3 0HE, UK
[3]Dept. of Electronics and Information Systems, Osaka University, 2-1, Suita, Yamada-oka, Osaka, Japan
[4]CREST, JST (Japan Science and Technology)
*TEL: +44 1223 467944, FAX :+44 1223 467942, E-mail : furuta@phy.cam.ac.uk

## 1. Introduction

Polycrystalline silicon (poly-Si) nanowires have been used as a building block for Coulomb-blockade (CB) devices. In these structures, individual silicon grains and grain boundaries (GBs) act as an electron charging island and a tunnel junction (TJ), respectively, and device operation has been reported for structures with less than a few nanometer grain sizes even at room temperature[1]. However, the properties of the GBs as TJs have not been studied in detail, and there has been no clear guideline to improve the GB-TJs for high temperature device operation.

We have recently reported a point-contact single-electron transistor (PC-SET) structure where both length and width of the channel are as small as the grain size in order to investigate electron transport properties via a few GBs. We have shown that the effective potential barrier height $V_B$ of the GBs ranges from 30 meV to 80 meV for as-deposited poly-Si [2]. In this work, we have investigated the relationship between properties of GB-TJs and the CB characteristics of the PC-SETs.

## 2. Fabrication of PC-SETs

We used a 50-nm-thick poly-Si film to fabricate PC-SETs. The poly-Si film was prepared by solid-phase-crystallization after $P^+$ implantation at 20 keV, $3x10^{14}$ $cm^{-2}$ as described in [2]. PC channel structures with two side gates were patterned on the poly-Si film layer with e-beam lithography. The channel dimensions were designed to be from 30 nm to 50 nm as shown in the inset of Fig. 1. Half of the PC-SETs were then oxidized at 1000 °C for 15 minutes. Scanning electron microscope (SEM) image of the Secco etched poly-Si film before oxidation is shown in Fig. 1, indicating that the grain size ranges from 20 nm to 150 nm.

## 3. CB properties of oxidized PC-SETs

As we reported previously [2], the as-deposited PC-SETs revealed nonlinear $I_{ds}$-$V_{ds}$ characteristics for about 1/3 of the fabricated devices. However, no CB oscillation was observed at a temperature above 4.2 K. In contract, the CB oscillations were observed for about 60 % of the oxidized PC-SETs although the CB oscillatory behavior varies largely among the devices.

Two typical $I_{ds}$-$V_{ds}$ characteristics and CB oscillations of the oxidized PC-SETs are shown in Figs. 2 and 3, respectively. Device A has much lower Coulomb gap and a shorter conductance oscillation period than those for Device B. It is apparent that size of the silicon grain responsible for the CB oscillation of Device B is much smaller than that of Device A. It should be noted that Device B has large zero-current CB region which is not clear in the Device A. The CB oscillation persisted up to about 40K in Device B.

Figure 4 shows the distributions of the GB potential barrier height $qV_B$ obtained for the PC-SETs with and without oxidation. $qV_B$ was extracted from the temperature dependence of resistivity at room temperature as described in [2]. The oxidation induces the increase of the average $qV_B$ by about 5 meV although the change in the $qV_B$ distribution is not significant. Nevertheless, the electrical characteristics changed after oxidation as shown by the CB oscillation, indicating that the GB tunnel barrier has been converted to oxide. As the oxidation of silicon at high temperature is limited by oxygen atom diffusion through GBs from device surfaces, the silicon oxide is expected to be sub-oxide, $SiO_x$ with $x<<2$. The extracted $qV_B$ is therefore supposed to show a band-offset between the $SiO_x$ and the crystalline silicon grains that is much smaller than that for the $SiO_2$/silicon interface. In fact, a larger $qV_B$ of more than 300 meV was also obtained for optimized oxidation condition: oxidized at a temperature less than 750 °C followed by annealing at 1000 °C.

Table 1 summarizes the Coulomb gap $V_T$, GB potential barrier height $qV_B$ and tunnel resistance $R_T$ derived from Device A and Device B. It shows that the ON/OFF ratio of Device B is much higher than that for Device A as both larger $V_B$ and $R_T$. This means that the larger $R_T$ is responsible mainly for the improved ON/OFF ratio. If there exists two TJs in the channel, the tunnel resistance per TJ for Device A is estimated to be about only $4R_Q$ ($R_Q$=26 kΩ) from the $R_T$ of 190 kΩ (see Tab. 1). This is not large enough to achieve good electron confinement. Assuming a rectangular potential for a TJ, $R_T$ is approximately given by the tunnel barrier height $V_B$ and thickness $d$ as [4]

$$R_T \propto V_B \exp\left(2d\sqrt{V_B}\right).$$

Provided $d$ is same value for Device A and B, $R_T$ for Device B would be about eight times larger than that for Device A. However, $R_T$ extracted for Device B is smaller than this theoretical estimate. This fact indicates that $d$ is not uniform among GBs, and $d$ for Device B is larger than that for Device A. In fact, we have observed by using high-resolution TEM that $d$ varies locally in the poly-Si film.

## 4. Conclusion

We have shown that the oxidation process of poly-Si PC-SETs results in the increase in both the barrier height and tunnel resistance of GBs, leading to appearance of CB effects. We have discussed conversion of the GBs to silicon sub-oxide tunnel barriers as a possible cause. More precise

control of the oxidized GB-TJ properties remains as a future issue to achieve uniform poly-Si SET operation.

## 5. Acknowledgments

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References

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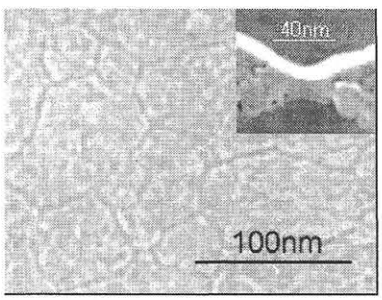


Fig. 1. Scanning electron microscope (SEM) image of as-prepared poly-Si film. The inset shows SEM image of a point-contact single-electron transistor (PC-SET) fabricated before oxidation process. The film thickness of poly-Si should be reduced to be about 18 nm after oxidation as reported in ref. 3.

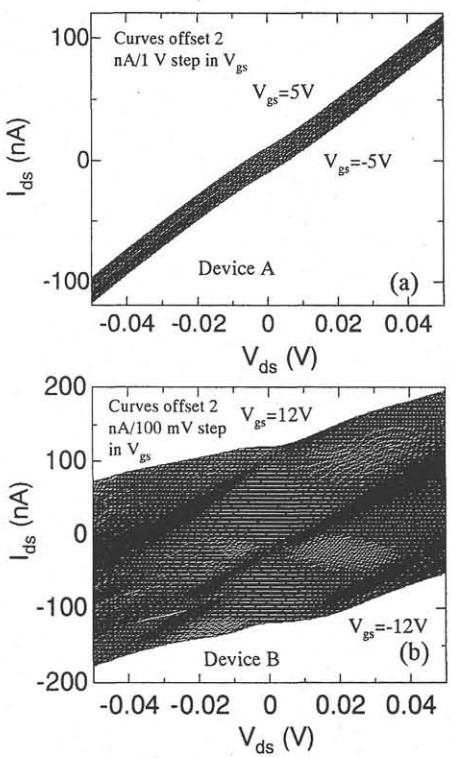


Fig. 2. Source-to-drain current-voltage ($I_{ds}$-$V_{ds}$) characteristics of oxidized PC-SETs with varying side-gate bias ($V_{gs}$). Device A was measured at 4.2K and Device B was measured at 9.0K. Each curve is shifted properly.

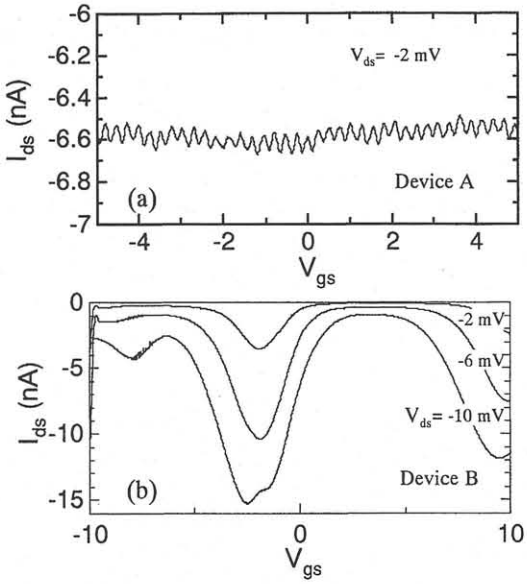


Fig. 3. Coulomb-blockade (CB) conductance oscillation for Device A and Device B. Device A was measured at 4.2 K and Device B was measured at 9.0 K

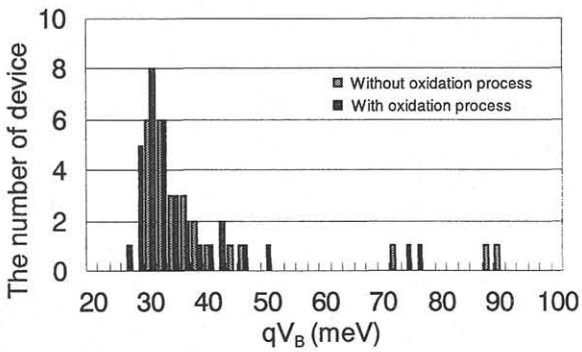


Fig. 4. Distribution of grain boundary potential barrier height $qV_B$ for the devices with/without oxidation. $qV_B$ are derived from temperature dependences of conductance around room temperature.

Table 1. Summary of oxidized PC-SETs property. ON/OFF ratio are defined as peak-to-valley ratio of $I_{ds}$-$V_{gs}$ characteristics at $V_{ds}$=2 meV and Oscillation periods are extracted by using Fast Fourier Transform (FFT).

| | Device A | Device B |
|---|---|---|
| Coulomb gap (meV) | 2.9 | 40 |
| ON/OFF ratio | 1.009 | 116 |
| Oscillation period (V) | 0.19 | 12 |
| Tunnel barrier (meV) | 36.4 | 87.6 |
| Tunnel resistance (Ω) | $2.89\times10^5$ | $1.01\times10^6$ |