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Charge Injection Characteristics of a Si Quantum Dot Floationg Gate in MOS Structures

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1. Introduction

The application of a silicon quantum dot (Si-QD) to floating gate MOS memories has been attracting much attention because of its multivalued capability[1, 2]. For MOS structures with a Si-QD floating gate[3, 4], we have confirmed the memory operations at room temperature. Also, we have demonstrated that multiple-step charging in the Si-QD floating gate to a level of about one electron per dot[4].

In this paper, to gain a better understanding of the multiple-step charging mechanism, we focus on the charge injection characteristics in MOS capacitors with a floating gate consisting of doubly-stacked Si-QD layers.

2. Fabrication of Si-QD Floating Gate MOS Capacitors

Hemispherical and single-crystalline Si-QDs were self-assembled on 3.5nm-thick SiO_2 by controlling the early stages of LPCVD of pure SiH_4 at 600°C [5]. After the formation of the first Si-QD layer, a ~1nm-thick thermal oxide layer was grown at 800°C in O_2 ambient of 8 Torr, and the second Si-QD layer was deposited under the same conditions. The average dot height and the total dot density evaluated by AFM were 5nm and ~4.6×10^{11} cm^{-2}, respectively. The surface of the second Si-QD layer was also covered with ~1nm-thick thermal oxide. Subsequently, a 3.3nm-thick amorphous Si layer was grown over the dot layer by LPCVD at 440°C, and fully oxidized in dry O_2 at 1000°C to form a 7.5nm-thick control oxide conformally. Finally, Al gate with a typical diameter of 1mm was fabricated by thermal evaporation.

3. Results and Discussion

The capacitance-voltage characteristics of a Si-QD floating gate MOS capacitor measured at room temperature at a gate voltage scan rate of 50 mV/s in the range between -3 and +3 V is shown in Fig. 1. The hysteresis originating from the electron charging and discharging of the QD floating gate is clearly observed and explained simply by the flat-band voltage shift of 0.76V. The transient current due to electron charging or discharging of the QD floating gate is also measured at 20 mV step with different delay times as shown in Fig. 2(a). Obviously, the current measured for the case of a 5s delay time is less than that of 1s delay time and current bumps are observable. Differential current (dI/dV) peaks around gate voltages of -0.9, -0.5, +0.8 and +2.6V (Fig. 2(b)), which were observed for a delay time of 1s swept over the range from -3 to +3V, confirm the multiple-step electron charging. The result of Fig. 2(b) is associated with not only the Coulomb blockade at QDs and from neighboring charged QDs[4] but also the shift of the

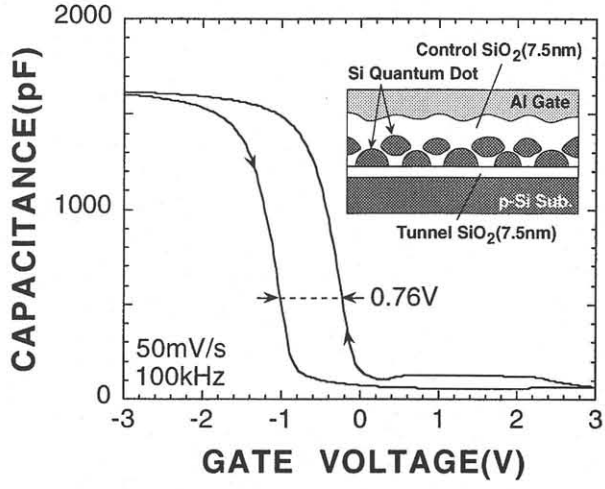

Fig. 1 Current-voltage characteristics of a Si QD floating gate MOS capacitor measured at room temperature. The scan rate of gate voltage and the frequency were 50 mV/s and 100 kHz, respectively.

charge centroid in the gate oxide during the electron charging to the Si-QD floating gate as described later.

In order to get a clear insight into charge injection characteristics in the Si-QD floating gate, temporal change in the current at V_G=+3V was measured after discharging of the QD floating gate as shown in the Fig. 3. The current drops just after applying gate bias and gradually increases until 30s. And then, the current rapidly increases and a distinct current peak is observed around 45s. After the current peak, an exponential current decay is obtained as seen in the typical charging characteristics of a capacitor. This unique transient current is interpreted in terms that the electric field distribution in the gate oxide is changed by shifting the charge centroid towards the control gate oxide in the doubly-stacked Si-QD floating gate. The following mechanism seems to be responsible for it. Initially, the electron injection in the 1st Si-QD layer decreases the electric field in the tunnel oxide between the substrate and the first QD layer, resulting in suppression of electron tunneling into the 1st QD layer. Because of larger charging energy of the 2nd Si-QD layer than that of the 1st Si-QD layer, when the 1st QD layer is sufficiently charged and the potential of the 1st QD layer becomes high enough, electrons can tunnel into the 2nd QD layer from the 1st QD layer. The electron tunneling from the 1st to the 2nd QD layer induces the recharging of the 1st QD layer. Because of these tunneling processes, the transient current is not decayed monotonously as represented in Fig. 3. It is likely that the observed current peak corresponds to the

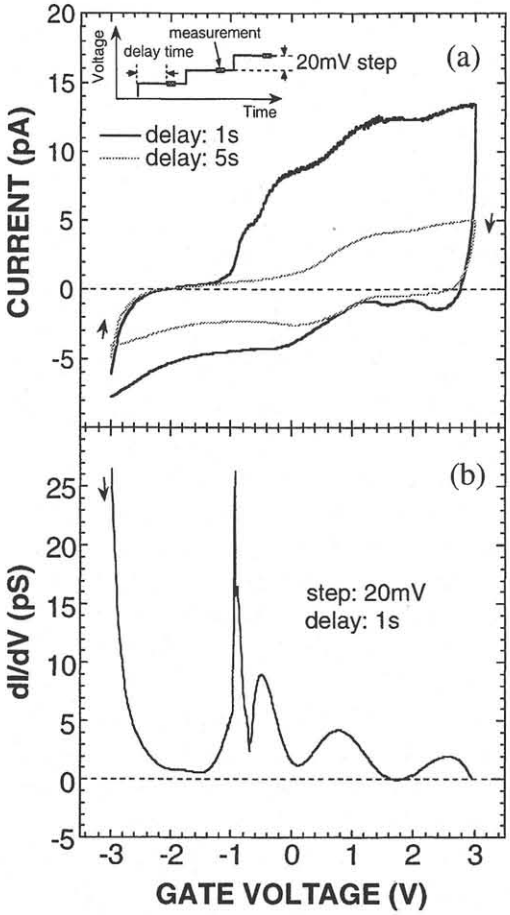

Fig. 2 Current-voltage characteristics of a Si QD floating gate MOS capacitor(a) and differential current(dI/dV) obtained for a delay time of 1s swept over the range from -3 to +3V(b).

electron tunneling from the 1st dot to the 2nd QD layer together with the recharging of the 1st QD layer. Figure 4 shows the transient current due to the recharging of the QD floating gate, which was measured at a gate voltage of V_G=+3V followed by holding at 0V for a certain time after the Si-QD floating gate was precharged at +3V. The fast current decay just after applying the gate bias and then the current peak are observable for each hold time at 0V although the time for the current peak is much shorter than the completely-discharged case (see Fig. 3). When the hold time at V_G=0V gets longer, the current peak appears later and becomes broader, and the total amount of reinjected electrons estimated from the time integration of the current is increased. Since the electrons stored in the QD floating gate is partially discharged during holding at Vg=0V, it takes a longer time to increase the potential of the 1st Si-QD layer for the case with a longer hold time and the broadening of the current peak could be attributed to the charge distribution in the partially-discharged QD floating gate.

4. Conclusions

The multi-step electron charging to a floating gate made of doubly-stacked Si-QD layers in the MOS capacitors has been demonstrated at room temperature. The transient current peak during the electron charging to the floating gate is indicative of the electron tunneling from the 1st to the 2nd QD layer.

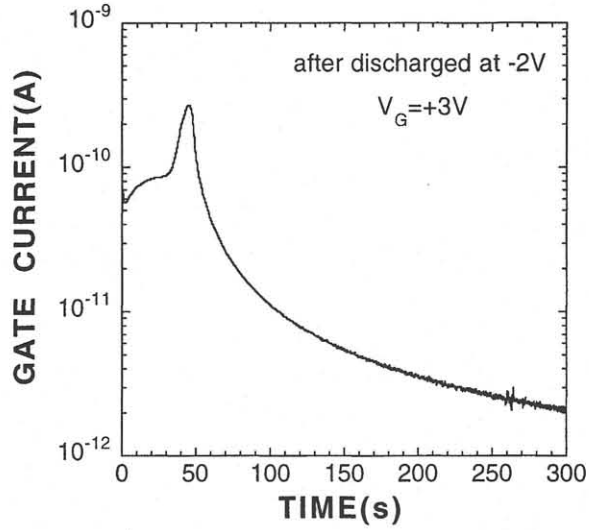

Fig. 3 Temporal change in the current of a Si QD floating gate MOS capacitor at V_G=+3V measured after discharging of QD floating gate.

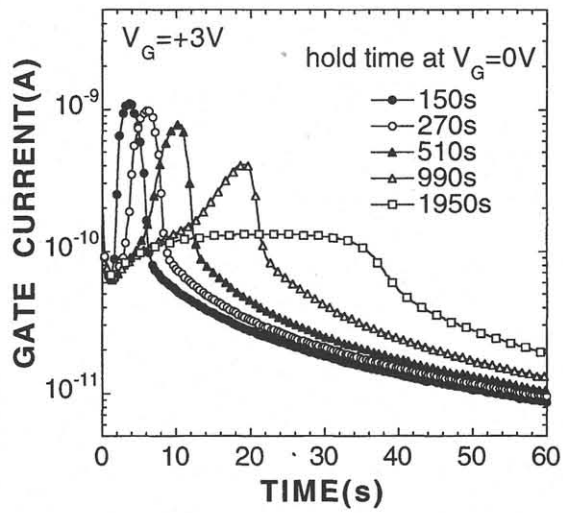

Fig. 4 Temporal change in the current at V_G=+3V measured after charging of the QD floating gate at V_G=+3V and hold at 0V. The hold time at 0V was changed from 150 to 1950s.

Acknowledgment

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