Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, Tokyo, 2001, pp. 548–549

D-7-1

A Merged SET-MOSFET Logic for Interface and Multiple-Valued Functions

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1. Introduction

Single-electron transistors (SETs) are attractive for logic and memory applications, since it works in smaller dimensions and with less power consumption. However, smaller voltage gain, smaller output resistance, and lower applicable voltage have limited its application.

Here, we propose a merged SET-MOSFET logic that can circumvent the above problems, achieving a voltage gain and output amplitude much larger than those of the conventional SET circuit.

2. Principle of Operation

Figure 1 shows schematics of the conventional SET inverter (a), and the merged SET-MOSFET inverter (b). For the conventional inverter, a constant-current load gives maximum voltage gain that is less than C_g/C_d. Output voltage V_{out} is negatively fed back to the potential of the Coulomb island through C_d, and this limits the gain. For realization of the Coulomb blockade condition, V_{out} is also limited to e/C_Σ, where e is elemental charge and C_Σ is the total capacitance around Coulomb island.

In the proposed circuit [Fig. 1(b)], a MOSFET is used to keep the SET drain voltage almost constant at V_{gg}-V_{th}, where V_{th} is the MOSFET threshold voltage. Since the drain voltage of a SET is not much affected by V_{out}, the negative feedback is suppressed, and large voltage gain and output amplitude can thus be obtained.

3. Experiments

The above idea was verified with a SET fabricated by the pattern-dependent oxidation (PADOX) process [1] and a MOSFET on the same wafer. In the measurements, a SET with gate capacitance of 0.27 aF, source/drain capacitance of 2.7 aF and tunneling resistance of 80~220 kΩ was used [Fig. 2]. An n-type MOSFET with effective channel width of 12 μm, channel length of 14 μm and gate oxide thickness of 90 nm was combined with the SET. Threshold voltage V_{th} corresponding to I_d=4.5 nA and V_{ds}=3 V was 1.07 V, and transconductance G_m at V_{ds}=V_{gs}=3 V was 151 μS. All the devices were operated and measured at 27 K.

Figure 3 shows the input-output characteristics of the conventional SET inverters. As is expected from the capacitance parameters, maximum voltage gain is as small as 0.1, and the output amplitude is only about 20 mV.

The same SET was combined with the MOSFET to make the SET-MOSFET inverter, and the characteristics are shown in Fig. 4. Originally, the SET I_d-V_{gs} characteristics have a large V_{ds} dependence as indicated in Fig. 2, and this V_{ds} dependence is alleviated by the MOSFET. When the SET I_d-V_{gs} curve selected by the V_{gg} setting crosses the load line I_o, the output switches between high and low levels as is seen in Fig. 4(a). Owing to the reduced negative feedback from V_{out}, high voltage gain of more than 40 is achieved.

Figure 5 is the equivalent circuit of the SET-MOSFET inverter. From the figure, V_{out} is given by

$$\begin{aligned} V_{out} &= -G_{m(SET)}R_{d(SET)}V_{in}+G_{m(MOS)}R_{d(MOS)}V_{ds(SET)} \\ &= -G_{m(SET)}R_{d(SET)}(1+G_{m(MOS)}R_{d(MOS)})V_{in}. \end{aligned}$$

This means that the SET gain is simply multiplied by the MOSFET gain, $G_{m(MOS)}R_{d(MOS)}$, if it is much larger than unity.

One of the main applications of the SET-MOSFET logic is a SET-to-CMOS interface circuit. Table 1 compares the various interface circuits proposed up to now. The merged SET-MOSFET logic is simple in terms of the number of elements and signal lines, and the V_{th} control of the MOSFET is relative and not so stringent.

The SET-MOSFET logic also has multiple-valued functions. The input-output characteristics shown in Fig. 4(a) can readily be used as a literal gate, which is a basic element of multiple-valued logic [2]. When the input and output terminals are shorted, the SET-MOSFET inverter has 2-terminal multipeaked negative resistance characteristics as shown in Fig. 6. This can work as a multiple-valued memory if an appropriate load device like a constant-current source is connected.

4. Conclusions

A merged SET-MOSFET logic is introduced that features large voltage gain and output amplitude far exceed the limits of C_g/C_d and e/C_Σ inherent to SET. It is suitable for a SET-to-CMOS interface circuit, and is also useful as a basic element for multiple-valued functions.

Acknowledgments

We thank Dr. Yukinori Ono for helpful discussions, and technical advice in electrical measurements.

References

[1] Y. Takahashi et al., IEEE Trans. Electron Devices, 43, 1213 (1996)

[2] L.Z. Micheel, *Proceedings of the 22nd International Symposium on Multiple-Valued Logic* (1992) p. 18.

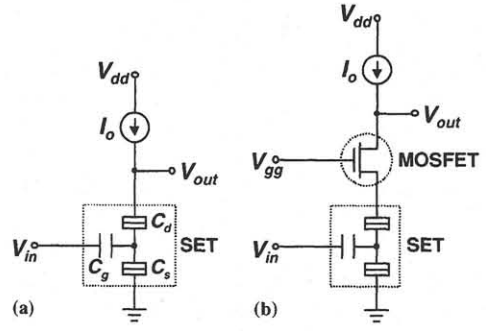


Fig. 1 Schematics of conventional SET inverter (a), and merged SET-MOSFET inverter (b) with a constant-current load I_o.

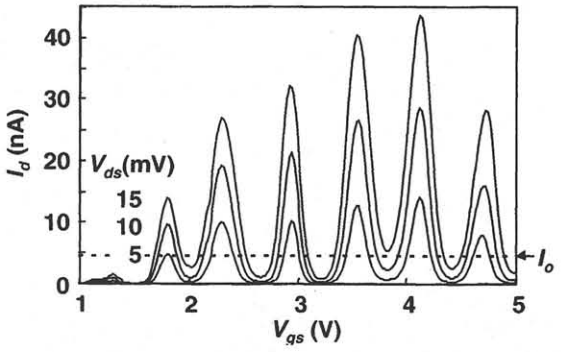


Fig. 2 I_d-V_{gs} characteristics of a SET fabricated by the pattern-dependent oxidation (PADOX) process [1], measured at 27 K.

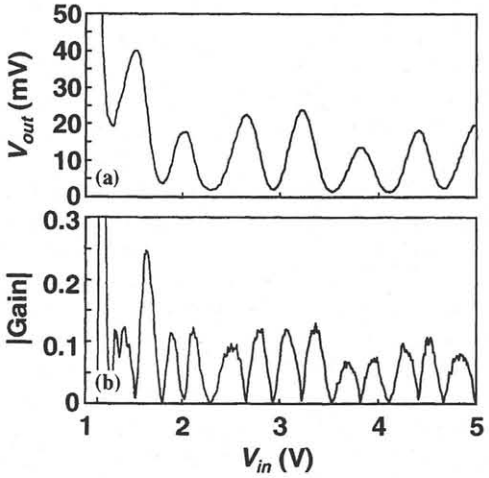


Fig. 3 Input-output characteristics of the conventional SET inverter [Fig. 1(a)] with a current load of 4.5 nA.

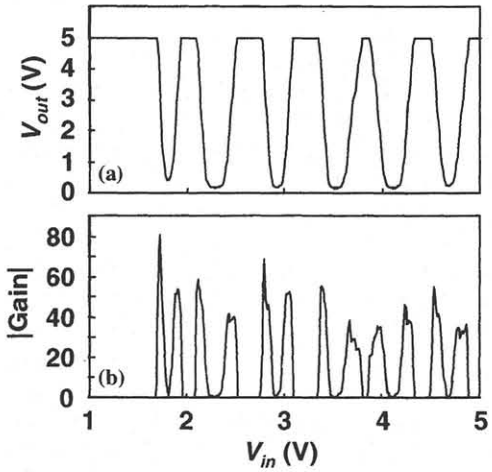


Fig. 4 Input-output characteristics of the merged SET-MOSFET inverter [Fig. 1 (b)] with V_{gg} of 1.08 V and a current load of 4.5 nA. The SET and the MOSFET are fabricated on the same SOI wafer.

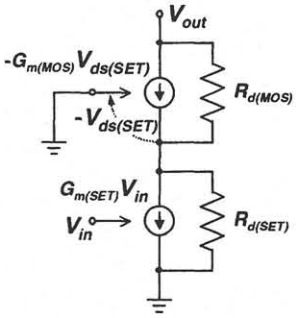
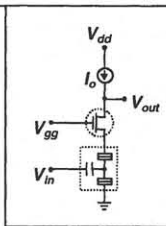
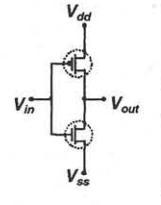
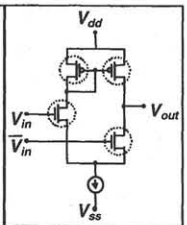


Fig. 5 Equivalent circuit of the merged SET-MOSFET inverter with a constant-current load [Fig. 1(b)].

Table 1 Comparison of SET-to-CMOS interface circuits.

Circuit Type			
	Merged SET-MOSFET Logic (This Work)	Inverter Amp.	Differential Amp.
No. of Elements	3	2	5
MOSFET V_{th} Control	Less Tight (relative accuracy*)	Tight (absolute accuracy)	Less Tight (relative accuracy)
Input Signal	Single	Single	Differential Pair
Multivalued Functions	YES	NO	NO

*If V_{gg} is supplied by the reference circuit consisting of the same SET and MOSFET.

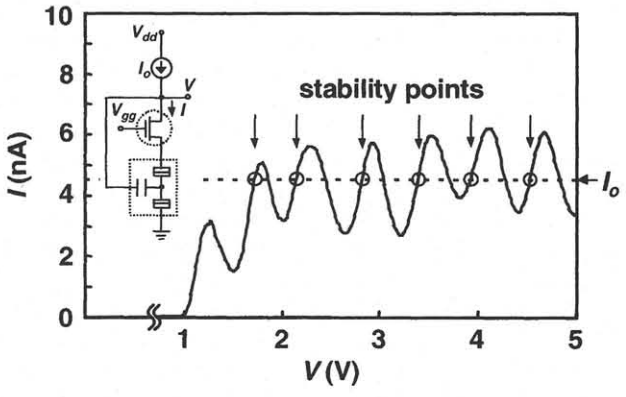


Fig. 6 Multipeaked negative resistance characteristics of the merged SET-MOSFET inverter with its input and output terminals shorted. If a current load of 4.5 nA is connected, six stability points appear, and the circuit works as a multiple-valued memory.