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Observation of Negative Differential Conductance and its Impact on Single-Electron-Transistor Characteristics

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1. Introduction

Recent progress in the research of Si single-electron transistors (SETs) has enabled us to make SETs operate at very high temperatures. As the operation temperature raises in accordance with making the dot smaller, quantum size effects on the conductance properties become more effective. Therefore, investigating the electronic structure of the dot and its interaction with the leads is quite important for proper control of SET characteristics. We have investigated the conductance of Si SETs in detail and found a new type of conductance anomaly displaying a negative differential conductance (NDC) in the drain current vs. drain voltage curves. We discuss its origin and the impact on the SET characteristics from the viewpoint of integrated-circuit applications.

2. Observation of Negative Differential Conductance

For the experiments, we used high-gain SETs [i.e., SETs whose gate capacitance (typically 2-3 aF) is larger than their junction capacitances (typically ~1 aF)], fabricated using vertical pattern-dependent oxidation [1,2]. All the measurements were done at 25 K with the source grounded. Figure 1(a) shows the drain current (I_D) vs. gate voltage (V_G) curve, while Fig. 1(b) shows the contour plot of the differential conductance (dI_D/dV_D) in a drain voltage (V_D) - V_G plane. The contour plot of the (dI_D/dV_D) shown in Fig. 1(c) was obtained by exchanging the source and drain terminals. NDC is observed in the regions indicated by the arrows in Figs. 1(b) and (c). Similar NDC was observed for several different SETs with the same fabrication design. The contour plot for another SET is shown in Fig. 2. I_D - V_D curves for a fixed V_G are shown in Fig. 3.

Noteworthy is that the present NDC is different from that observed previously in a Si SET [3], and can not be explained by the proposed model in which the band structure of the emitter, i.e., of the lead from which electrons are injected to the dot, play a key role. The distinctive nature of the present NDC is that the regions where NDC appears align in parallel with the longer rising sides of the diamonds, independent of which tunnel junction is connected to the drain [as shown in Figs. 1(b) and (c)]. This indicates that the phenomenon is related to the electrostatic conditions for tunneling at the drain junction, and therefore, the dot states and band structures of the lead at the drain side must play important roles.

We expect that the present finding relies on the use of the high-gain SETs. Since the high-gain SETs have a relatively large gate capacitance, electrostatic potential in the dot does not move so much during V_D sweeps because it is given by $C_D V_D / (C_D + C_S + C_G)$ where C_D , C_S , and C_G are the drain, source, and gate capacitances, respectively. Therefore, the present contour plot measurements are fairly good experiments for the tunneling spectroscopy of the electronic structures of the dot and of one side of the leads (i.e., the drain). The importance

of this asymmetric voltage sharing is also indicated by the fact that the appearance and disappearance of the NDC are strongly influenced by which side of the junctions is connected to the drain, as represented by the data shown in Fig. 2(b) where, in contrast to Fig. 2(a), no NDC is observed.

3. Impact on the SET Characteristics

NDC has already been obtained in other quantum devices like resonant tunneling diodes, and its application to static memories and logic elements has been widely discussed. A prominent feature of the present NDC is that it can be controlled by the gate. This gives a new function to the devices. Figure 4(a) shows the contour plot of the drain current for the SET shown in Fig. 1. [The corresponding dI_D/dV_D contour plot is Fig. 1(b)]. In this plot, the conductance anomaly results in abnormally winding constant-current curves. In the NDC regions marked by the arrows, the inverting voltage gain of the SETs [4] is no longer defined, or it can be said that it is infinite. Alternatively, the output voltage at the drain for a constant drain current bias forms a hysteresis loop as shown in Fig. 4(b). This characteristic is directly applicable to a Schmitt-trigger-type inverter. The transfer curve of the Schmitt-trigger inverter [5] is schematically shown in Fig. 5. This inverter has two thresholds (V_{TH-LOW} and $V_{TH-HIGH}$) depending on whether the input is changing from LOW to HIGH or from HIGH to LOW. Owing to this hysteresis, the inverter has excellent noise immunity because once the output is LOW, it will not go HIGH again until the input is decreased to the level of V_{TH-LOW} , and vice versa. In conventional MOS circuits, this inverter is constructed by using an internal feedback and thus requires a complicated circuit. The transfer curve in Fig. 5 is what we see in Fig. 4(b), indicating that we can construct this inverter using just one SET. In single-electron ICs, this type of circuit would be essential because single-electron devices are very sensitive to noise.

4. Conclusions

A new type of conductance anomaly resulting in NDC has been observed for Si SETs. The data indicate that the electronic structure of the dot and its interaction with the lead at the drain side play important roles. In addition, we have proposed the application of the finding to a Schmitt-trigger-type inverter, which promises to be a key device in single-electron circuits because of its excellent noise immunity.

References

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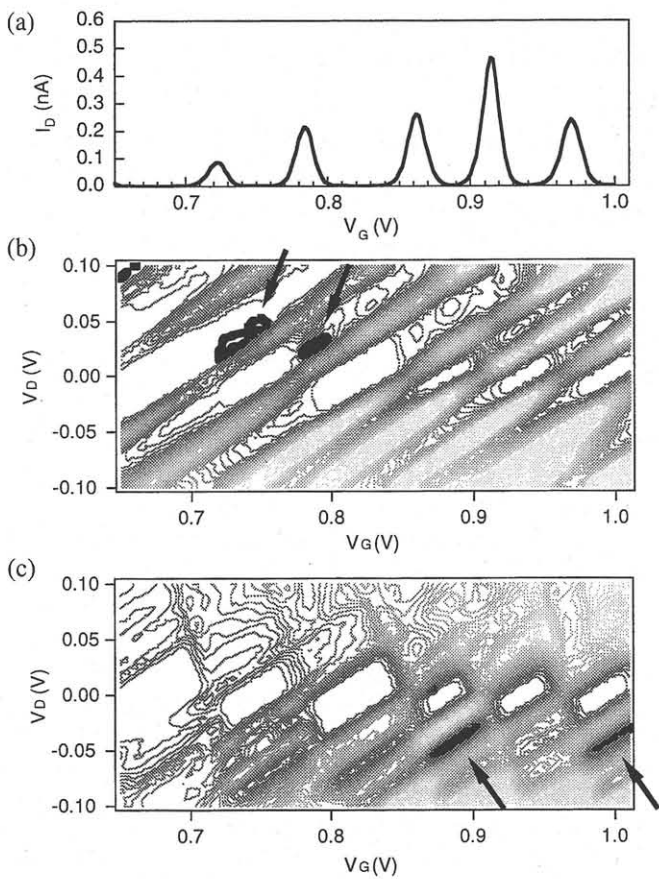


Fig. 1. Drain current vs. gate voltage characteristics with a drain voltage of 10 mV (a) and contour plots of dI_D/dV_D (b) and (c). In the measurements for (c), the source and drain terminals were exchanged from those for (a) and (b). For all the measurements, the source was grounded. The dark areas marked by the arrows exhibit NDC.

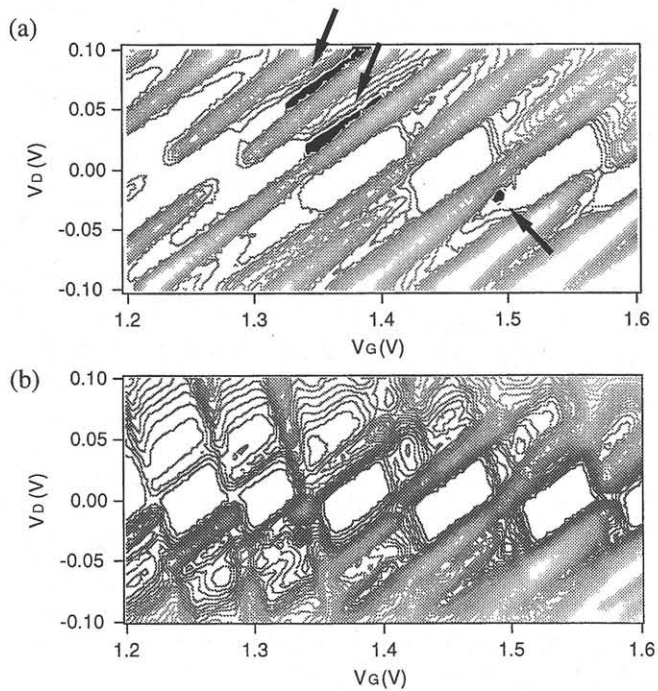


Fig. 2. dI_D/dV_D contour plots. In the measurements for (b), the source and drain terminals were exchanged from those for (a). For both measurements, the source was grounded. The dark areas marked by the arrows exhibit NDC. In (b), no NDC is observed.

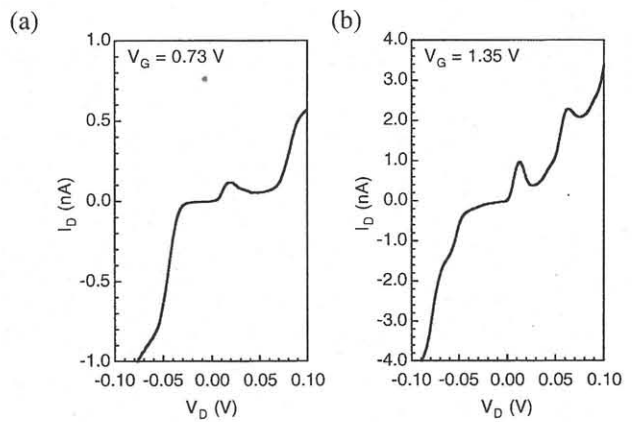


Fig. 3. Drain current vs. drain voltage curves for a fixed gate voltage. The corresponding dI_D/dV_D contour plot is Fig. 1(b) for (a) and Fig. 2(a) for (b). The fixed gate voltages are 0.73 V for (a) and 1.35 V for (b).

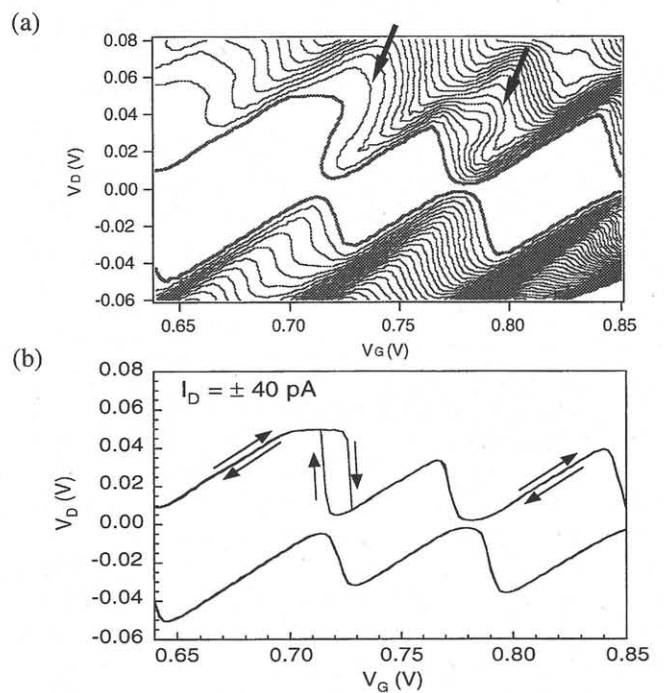


Fig. 4. Contour plot of drain current (a) and drain output-voltage for a constant drain current of ± 40 pA (b). The corresponding dI_D/dV_D version of the contour plot is Fig. 1(b). In (a), the contour lines are drawn with an increment of 40 pA, and two bold curves are the contour lines for $I_D = \pm 40$ pA. The areas marked by the arrows are the NDC regions shown in Fig. 1(b). In (b), the arrows indicate the directions for the V_G sweep.

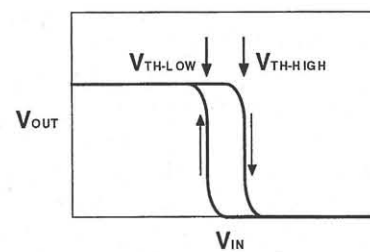


Fig. 5. The transfer curve of the Schmitt-trigger inverter. V_{TH-LOW} and $V_{TH-HIGH}$ denote lower and higher threshold voltages, respectively.