

**D-7-3****Single Electron Transistors with Sidewall Depletion Gates on a Silicon-On-Insulator Nano-Wire****Kyung Rok Kim, Dae Hwan Kim, Suk Kang Sung, Jong Duk Lee, Byung Gook Park**

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**I. Introduction**

Single electron transistors (SETs) are promising candidates for future functional devices because of their high integration density and low power consumption. For an application of SETs as components of the integrated circuitry, there have been two issues. One is the process compatibility with conventional VLSI technology. To evaluate the usefulness of the SET-CMOS hybrid scheme [1], it is strongly required that SETs should be fabricated by the conventional VLSI technology. The other issue is the predictability of SET characteristics. From this viewpoint, a structure with an electrically induced quantum dot has a promise for an optimization of the device characteristics [2,3].

In this work, novel SETs with sidewall depletion gates on a SOI wire are demonstrated, using conventional silicon (Si) VLSI technology. The uniform wire and sidewall gates form an electrostatically well-defined quantum dot and eliminate the possibility of unintended quantum dot formation.

**II. Device Structure and Fabrication Process.**

SETs fabricated on a SIMOX (separation by implanted oxygen) *p*-type (100) wafer are schematically shown in Fig. 1. Uniform 30-nm-wide SOI wire was formed by the sidewall patterning technology [4], which effectively suppressed unintentional potential barriers. After the deposition of the oxide, nitride groove was lithographically defined and thermal oxidation was done at 800°C. Then, 40-nm thick *n*-type highly doped polycrystalline silicon (poly-Si) was deposited and anisotropically etched in Cl<sub>2</sub> reactive-ion plasma, forming a poly-Si sidewall depletion gates. After the deposition of the control gate oxide, the poly-Si control gate was defined by the conventional lithography. The fabricated device structure with geometry parameters is shown in Fig. 2. Inversion layer in a 45-nm-thick SOI wire is formed by the back gate bias ( $V_{BG}$ ), and two tunnel junctions are formed by poly-Si sidewall depletion gate bias ( $V_{SG}$ ). Charge of electrically induced quantum dot is controlled by the poly-Si control gate bias ( $V_{CG}$ ). Figure 3 show SEM images of 30-nm-wide SOI wire and poly-Si sidewall depletion gate.

**III. Electrical Characteristics**

The fabricated device has geometric parameters (Fig. 2.), which are  $W_{CH}$  (the width of SOI wire) = 30 nm,  $T_{OX}$  (the thickness of control gate oxide) = 60nm,  $W_{SG}$  (the width of sidewall gate) = 40nm,  $S_{SG}$  (the separation between two sidewall gates) = 185nm, and  $L_{CH}$  (the length of SOI wire) = 7 $\mu$ m.

Fig. 4 shows  $I_{DS}$ - $V_{CG}$  characteristics of the fabricated SET at 4.2K. The coulomb oscillation period ( $\Delta V_{CG}$ ) is 80mV and the extracted  $C_{CG}$  from this period is 2.0aF. The estimated  $C_{CG}$  is 3.1aF from the geometric parameters since the control gate capacitance

$C_{CG}$  is the control gate oxide capacitance with the area of Si dot ( $S_{SG} \times W_{CH}$ ). The discrepancy is about 62% and this result from the reduction of effective dot area by the electric field effect and the increment of effective oxide thickness due to the inversion layer near Top Si/Box interface by  $V_{BG}$ .

Coulomb gap was observed in Fig 5. Nonlinear shape of drain current is clear, and Coulomb gap voltage at  $V_{CG}=20$ mV is about 40mV. The magnitude and position of coulomb gap is successfully modulated by  $V_{CG}$  according to the Coulomb blockade diagram based on orthodox single electron tunneling theory (Fig. 7.). These results indicate that the electrically induced quantum dot is well formed in the intentional spot and the fabricated SET shows intentional single-dot characteristics as we design.

Also, Fig. 4 shows constant oscillation period and clear multiple peaks as a function of increasing  $V_{CG}$ . It is consistent with 3-dimensional device simulation result in Fig. 6. As shown in Fig. 6, the depletion width is nearly constant when  $V_{CG}$  varied from 0.0 to 0.6V. This simulation result indicates that the electrically induced quantum dot of the fabricated SETs is not sensitive to the gate bias condition. These characteristics stem from 3-dimensional structure of the sidewall depletion gate wrapping SOI channel. Considering that the switching characteristics of the previously reported SETs based on the electrically induced quantum dot was degraded sensitively to the gate bias conditions, so that a few peaks was observed only in the subthreshold region [2,3], the fabricated SETs are much improved and comparable to SETs based on the physically formed quantum dot [5].

Moreover, the peak position is modulated by  $V_{SG}$  (Fig.4.) without additional electrodes and the voltage gain of SETs which is given as the ratio  $C_{CG}/C_D$  at a constant current is 1.3, larger than one (Fig.7.) These characteristics are promising properties for the integrated circuit application.

**IV. Conclusion**

We have fabricated novel SETs with sidewall depletion gates on a SOI nano-wire using sidewall patterning technology. The fabricated SETs show intentional single-dot characteristics, confirming the elimination of unintentional potential barriers in SOI nano-wire. Also, It shows multiple peaks with a constant period, overcoming the drawbacks of the previous SETs based on electrically induced quantum dots.

**Acknowledgments**

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**References**

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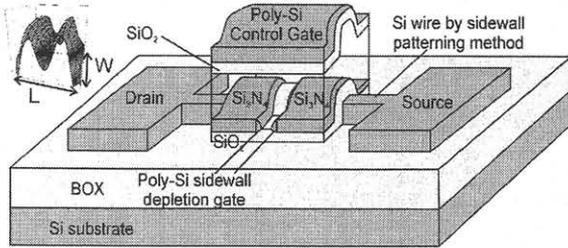


Fig. 1. Schematic diagram of the fabricated SET. Starting material was a 45nm thick SOI film. Inset shows the electron potential profile in SOI wire calculated by 3-dimensional device simulation.

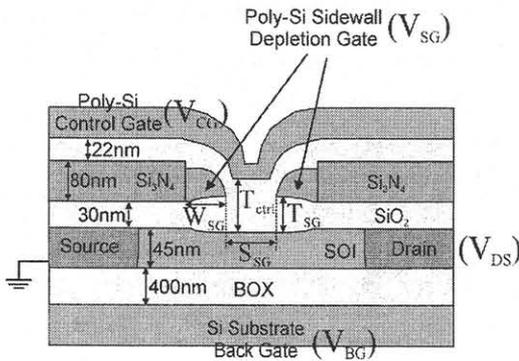


Fig. 2. Cross sectional view of SETs with sidewall depletion gates on an SOI wire.

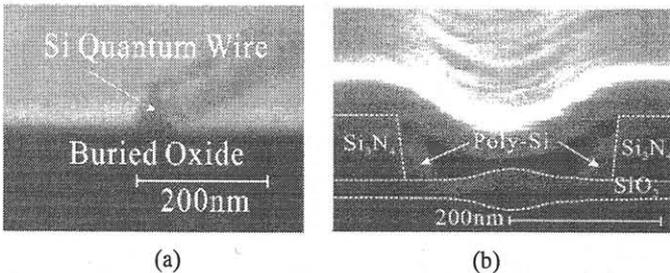


Fig. 3. SEM images of SOI wire and sidewall depletion gate (a) 30nm-wide SOI wire (b) Poly-crystalline silicon sidewall depletion gate.

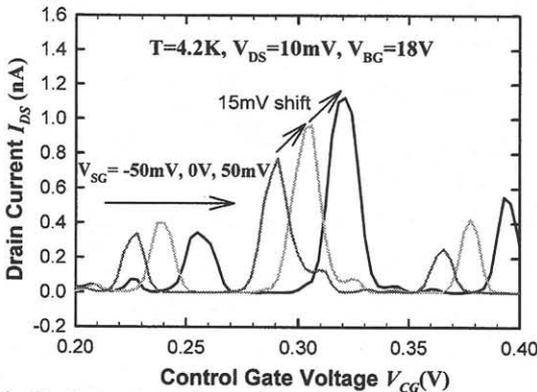


Fig. 4. Control gate voltage dependence of drain current as a function of  $V_{SG}$  of the fabricated SET at 4.2K

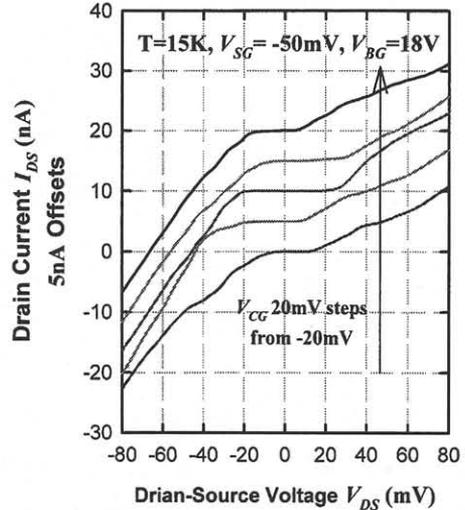


Fig. 5. Drain-Source voltage dependence of drain current of SET at 15K. Drain current is shown by offset of 5nA for a clarity.

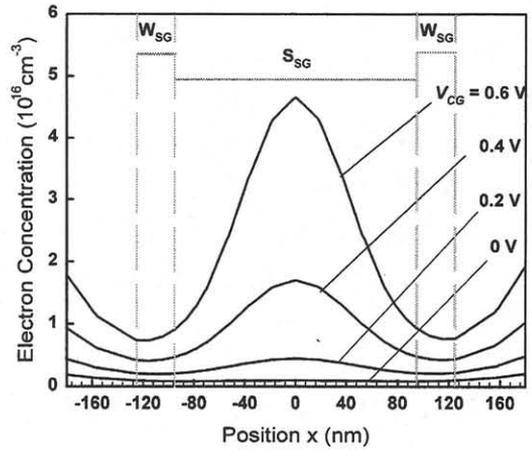


Fig. 6. Electron concentration along an SOI wire length direction at 7nm depth beneath Si/SiO<sub>2</sub> interface. Poisson equation is solved by 3-dimensional device simulator. The geometry parameters for simulation are:  $S_{SG}=185\text{nm}$ ,  $W_{SG}=30\text{nm}$ ,  $W_{CH}=30\text{nm}$ ,  $T_{\text{ctrl}}=60\text{nm}$ ,  $T_{SG}=38\text{nm}$ ,  $L_{CH}=2\mu\text{m}$ .

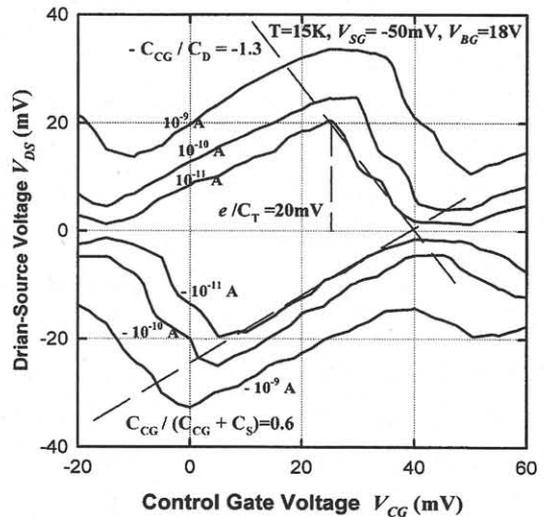


Fig. 7. Contour plot of drain current as a function of  $V_{CG}$  and  $V_{DS}$  at 15K.