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Room Temperature Coulomb Diamond Characteristic of Single Electron Transistor

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We have succeeded in getting the clear Coulomb diamond characteristics of the single electron transistor (SET) at room temperature. In order to obtain a clear Coulomb diamond characteristic at room temperature, the total capacitance of the SET should be less than ~0.5aF. For the reduction of the size of the SET, and the achievement of such a small capacitance, we have already proposed to use the single wall carbon nanotube atomic force microscopy (AFM) cantilever. Furthermore, we suggest hear another two technology to reduce the total capacitance of the SET, one is the alternation of the material of the substrate and the other is the annealing process. The substrate of the SET with the lower dielectric constant material can reduce the total capacitance of the SET. Figure 1 shows the dependence of the total capacitance on the dielectric constant of the substrate calculated by the three-dimensional simulation. From this simulation, it becomes clear that the total capacitance with the quartz (SiO_2) substrate is 1.5 times smaller than the Al_2O_3 substrate. However, the conventional quartz substrate is not suitable for the AFM nano-oxidation process, because of the high roughness of 1nm with the polishing scars. We have succeeded in obtaining the atomically flat quartz substrate by dissolving it in the 50% HF solution for 2 ~ 3hours. The step height is 0.38nm and the width of the terrace is as large as 360nm as shown in Fig. 2. The roughness of the terrace is about less than 0.2nm. The fabricated SET is heat-treated at 120 ~ 190 degrees Centigrade by the hot plate in air. This process can further reduce the island volume by the uniform oxidization of the Ti film from the surface close to the air.

The fabricated SET had one island between two tunnel junctions made by the TiOx barrier, and the gate electrode was formed on the backside of the Al_2O_3 substrate. The drain current versus drain bias characteristics at 7K and room temperature showed the Coulomb blockade about 2.0V at 7K, and 0.3V at room temperature, respectively, as shown in Fig. 3. Figure 4 shows the Coulomb diamond characteristic of the SET measured at room temperature. The gate bias was applied from -3V to 3V and the drain bias was changed from –0.45V to +0.45V. The three Coulomb diamond structures were observed. The contour graph of the Coulomb diamond characteristic was shown in Fig. 5. The Coulomb blockade area was changed periodically with increasing the gate bias. From the Coulomb diamond characteristic at room temperature, the ratio of the each tunnel junction capacitance was obtained that $C_1/C_2 = 0.52$. The period of the drain current oscillation was 2.5V. Therefore, the gate capacitance was founded to be $Cg = 0.064$aF, and the tunnel junction capacitances calculated by the orthodox theory were that $C_1 = 0.16$aF, and $C_2 = 0.309$aF. The calculated Coulomb energy, $e^2/2C_\Sigma$ where C_Σ was the total capacitance of the SET, was as high as 240meV, which was 9 times higher than the room temperature thermal energy of 26meV. The contour graph of the Coulomb diamond characteristic calculated by the orthodox theory using the parameters obtained from the experimental result was shown in Fig. 6. The calculated result well simulated the experimental results.

The clear Coulomb diamond characterice was obtained even at room temperature in our SET, because of the small capacitance of the order of 10^{-19}F attained by the various new technologies.

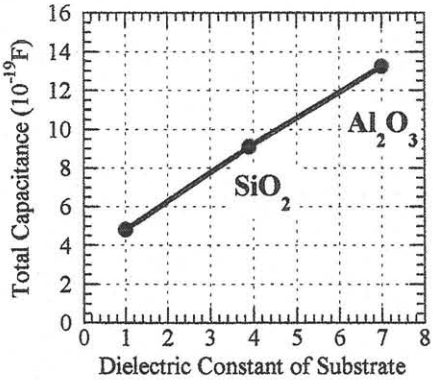

Fig. 1, Dependence of total capacitance of SET on dielectric constant of substrate.
Total capacitance of SET with SiO_2 substrate was found to be about half of that of Al_2O_3 substrate.

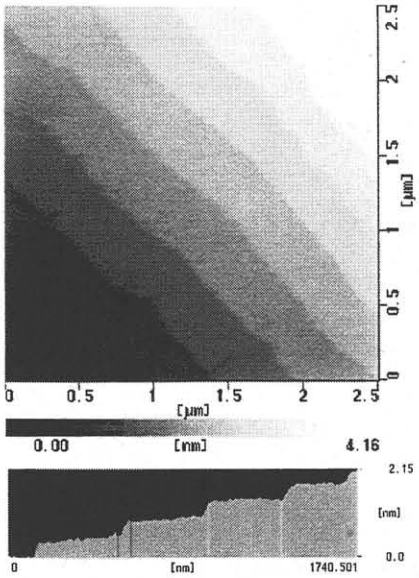

Fig. 2, AFM image of atomically flat quartz(SiO_2) substrate. Clear step lines was observed.
Width of terrace was as big as 360nm and roughness was about 0.2nm high.

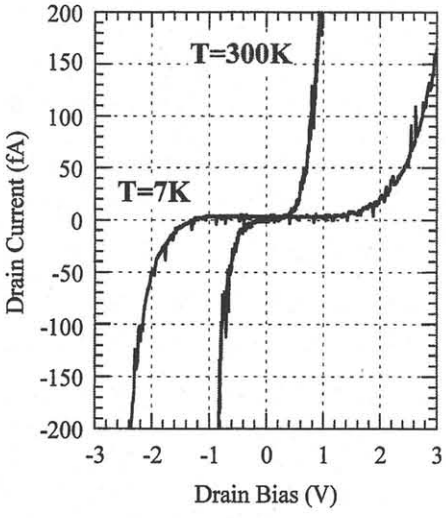

Fig. 3, Drain current versus drain bias characteristic at 7K and room temperature. Coulomb blockade was 2.0V at 7K and 0.3V at room temperature.

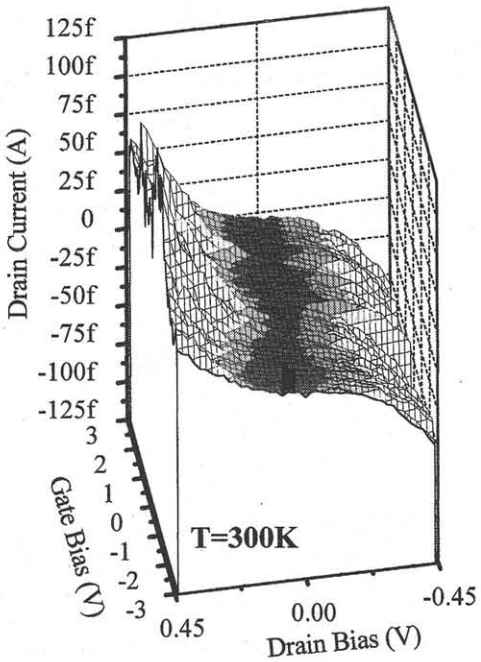

Fig. 4, Three-dimensinal Coulomb diamond characteristic of fabricated SET at room temperature.
Three Coulomb diamonds were obtained at V_G=-3V ~ +3V and V_D=-0.45V ~ +0.45V.

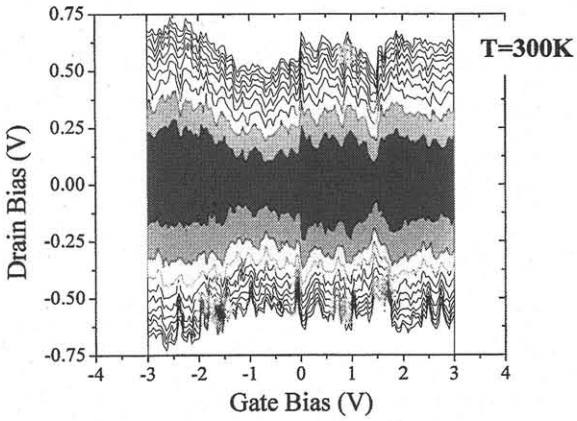

Fig. 5, Contour plot of Coulomb diamond at room temperature.
From slope of Coulomb diamond, tunnel junction capacitance C_1 was found to be about half of C_2

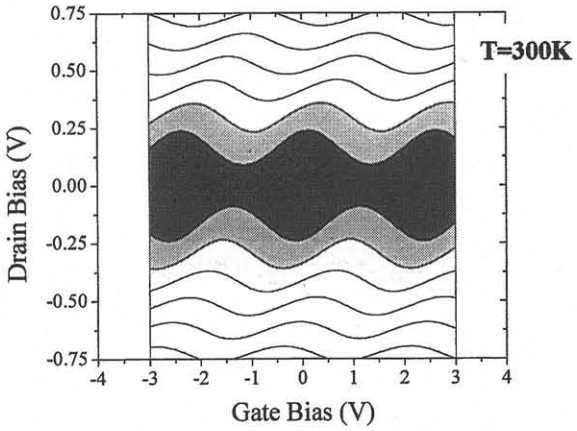

Fig. 6, Contour plot of Coulomb diamond calculated by orthdox theory. Tunnel junction capacitance of C_1=0.16aF, C_2=0.309aF and Gate capacitance of C_G=0.064aF were used obtained from experimental data of Fig. 5.