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DC Characteristics of InP HBTs under High-Temperature and Bias Stress

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1. Introduction

Previously, we investigated the stability of the emitter junction characteristics of InP/InGaAs heterojunction bipolar transistors (HBTs) under high-temperature and bias stress [1]. It was shown that the stability depends on the crystallographic orientation of the InP emitter mesa; promising results were obtained for devices whose orientation was parallel to the Primary Flat of the substrate. Unfortunately, the HBTs used for the initial work had poor current gain even before stressing (only ~10) and were not applicable to practical circuits. This problem was overcome by optimizing our device design, and we succeeded in obtaining HBTs suitable for 40 Gb/s ICs [2]. In this work, we again tested these HBTs to examine the dc degradation behavior in more detail. The HBTs showed various modes of degradation; however, these degradations appear to saturate with stress time and the saturation level is not serious in the device-operation bias range. Preliminary stress testing for frequency divider ICs was also carried out to examine the influence of the initial degradations on IC operation.

2. Device Structure and Fabrication

InP/InGaAs HBT epitaxial layers were grown on semi-insulating 3-inch InP substrate by MOVPE. The layer structure is almost the same as reported previously [2]. The emitter is InP doped with silicon and the base is InGaAs doped with carbon. The collector is 300-nm-thick InGaAs. We fabricated HBTs with a 6-μm^2 emitter. Benzocyclobutene (BCB) films were used for passivation. The fabricated devices exhibit current gain of 36.9±2.5, f_t of 123±2 GHz, and f_{max} of 186±4 GHz at J_C = 0.5 mA/μm^2 and V_{CE} = 1.2 V.

We also fabricated static 1:2 frequency divider ICs on the same epi-wafers. They consist of input and output buffers, a master-slave T-FF, and an output driver. The appropriate bias current is provided by internal voltage generators. On-wafer measurements showed the maximum operation frequency of 39.0±1.7 GHz at a supply voltage of V_{EE} = -4.5 V (I_{EE} ~ 200 mA).

3. Stress Tests and Results

Transistors

In the stress tests, HBTs were biased at V_{BE} = 0.72 V and V_{CB} = 0.5 V at an oven temperature of 180℃ with nitrogen ambient. Under these conditions, emitter current density was around 0.7 mA/μm^2. Shown in Fig. 1 is the change in collector current, base current, and current gain periodically monitored during the stress at 180℃. It is shown that current gain decreases gradually, and that the decrease is associated with an increase in base current. However, such degradation saturates within the first 100~200 hr and current gain of over 20 is maintained. After each current is stabilized from 200 to 500 hr, collector current then tends to increase while base current decreases slightly. Owing to this behavior, current gain recovers at around 1,000 hr.

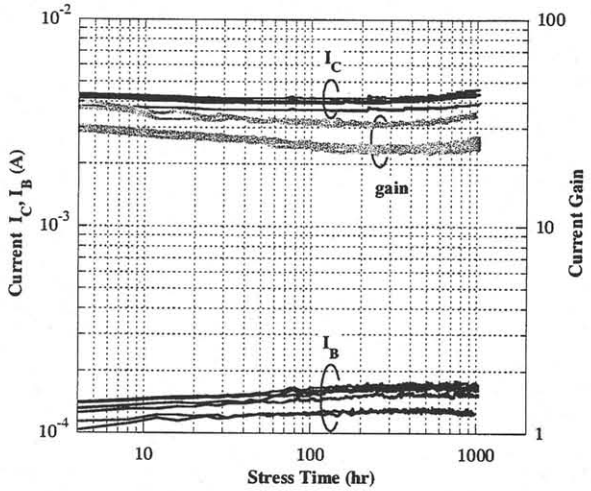

Fig. 1. Change of I_C, I_B, and current gain β during stress at 180℃.

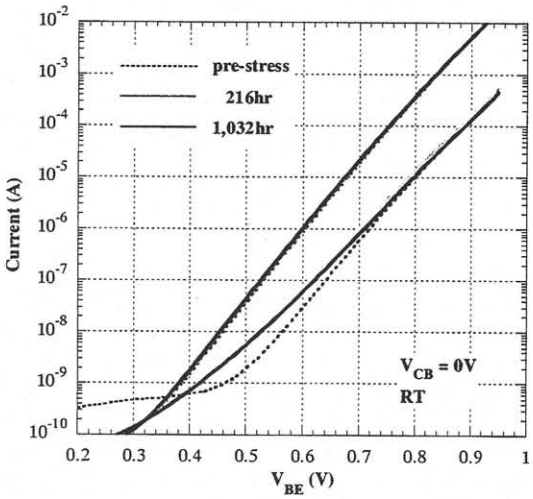

Fig. 2. Typical Gummel plots for the HBT before and after stress.

Figure 2 shows Gummel plots measured at room temperature after 216 hr and 1,032 hr of stress. There is an increase in base current in the low-bias region (V_{BE} < 0.7 V). Such non-ideal leakage current implies the degradation of crystal quality near the emitter mesa surface, which presumably gives the initial increase of base current observed in Fig. 1. In the operation bias range, however, serious gain reduction is not observed.

Figure 2 also shows a slight decrease in turn-on voltage (~5 mV at V_{BE} = 0.6 V) for the device stressed for 1,032 hr. This means that

the increase in collector current in Fig. 1 is associated with the shift in turn-on voltage. One possible explanation of this degradation mode is the diffusion of carbon interstitials and/or residual hydrogen from the base into the emitter.

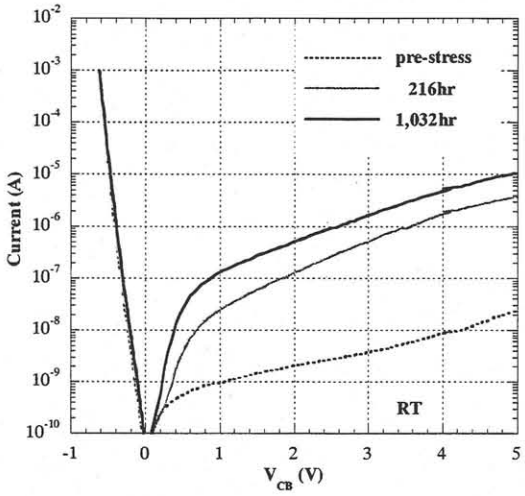

Fig. 3. Measured I-V characteristics for a base-collector diode.

We also investigated collector junction characteristics, which are shown in Fig. 3. There is a significant increase in reverse-biased leakage current within the first 216 hr of stress, but such increase saturates at 1,032 hr. This degradation behavior has also been reported by other groups [3]. Fortunately, the leakage current is less than 1 μA at V_{CB} < 2 V, much lower than the device operation current.

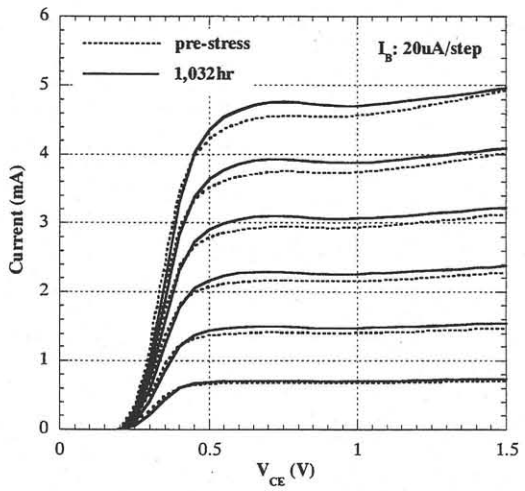

Fig. 4. I-V characteristics of the HBT before and after 1,032hr of stress.

Frequency Divider ICs

Figure 4 shows collector I-V curves for the HBT after 1,032 hr of stress. As expected from Figs. 2 and 3, serious degradation does not occur. Encouraged by this result, preliminary stress testing for frequency divider ICs was also performed. In the stress tests, four discrete IC chips were mounted and sealed in ceramic packages. They were biased at V_{EE} = -4.5 V at an oven temperature of 110℃. During the stress, output drivers performed external 50 Ω termination and input clock terminals were connected to ground terminals in order to eliminate the IC self-oscillation. The estimated substrate temperature was 175℃. Figure 5 plots the bias current, I_{EE}, as a function of stress time. Each divider yielded nearly constant bias current during and after the stress, and exhibited over-30-GHz operation after 991 hr of stress (even in the packaged condition). These results suggest that dc degradation observed for the tested HBTs has little impact on digital IC operation.

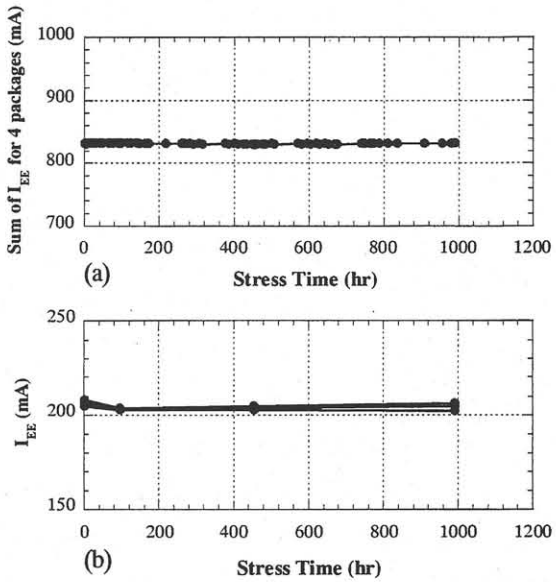

Fig. 5. Bias currents of static frequency dividers as a function of stress time; (a) sum of currents from four packages monitored during stress, (b) bias current for each divider IC measured at room temperature.

4. Conclusion

In summary, we have investigated dc degradation behavior of InP/InGaAs HBTs caused by high-temperature and bias stress. Major degradations observed in this work are as follows:

- Initial increase in I_B and resultant decrease in β
- Initial increase in reverse-biased collector current, I_{CO}
- Increase in I_C associated with lower shift in turn-on voltage

The initial degradations observed appear to saturate and are expected not to be fatal for IC operation, although longer-time stress testing is required to ultimately judge the stability of junction characteristics.

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References

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