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Robust 0.13-μm Gate HJFET with Low Fringing Capacitance

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1. Introduction

The millimeter-wave bands are attracting considerable attention, being suitable for focused-beam radars. GaAs-based heterojunction FETs (HJFETs) are widely used in millimeter-wave V- and W-bands. T-shaped gates with a length of around 0.1μm [1] are generally adopted to achieve a high-gain in millimeter-wave bands, although such an ultra-short gate is liable to peel off the semiconductor surface. To overcome this problem, gates are commonly embedded in a dielectric layer [2]. However, the dielectric layer increases the parasitic gate capacitance (for Cgs and Cgd) and adversely affects the high-frequency gain [3].

To meet the needs for both a high yield and high-frequency gain at the same time, we have been investigating a new gate structure, in which segments of the gate are supported by an embedding SiO_2 film, and the remainder is unsupported. This structure can be built using the fabrication process explained below, where the SiO_2 film around the embedded gates is partially removed along the fingers in a striped pattern.

2. Gate and Device Fabrication

The embedded gates with SiO_2 are first fabricated using the process flow [2] shown in Fig.1. A T-shaped gate opening is made by two-step dry-etching with a chemically amplified (CA) resist and EB lithography (Fig.1(a)-(c)). Thermally stable Au/WSi is sputter-deposited and dry-etched to form the T-shaped gate (Fig.1(d)-(e)). Finally, the SiO_2 around the gate is partially removed along the fingers in a striped pattern using buffered hydrofluoric acid (BHF). The resulting structure is shown in Fig.2.

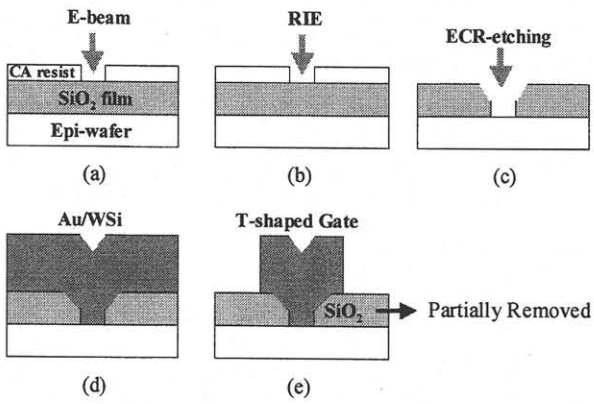

Fig.1 Process flow for T-shaped gate HJFETs

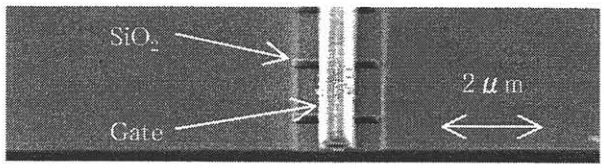

Fig.2 SEM view of the device structure

A schematic cross section of the fabricated device (embedded part) is shown in Fig.3 (Lg=0.13μm, Lgs=0.45μm, Lgd=0.55μm, and Hg=280nm). Epitaxial layers are grown by MOCVD on a 4-inch substrate. The epitaxial structure allows selective 2-step recess etching because it has an i-AlGaAs stopper / i-GaAs spacer layer under the n^+-GaAs ohmic-contact layer. The active part of the structure consists of an undoped $In_{0.20}Ga_{0.80}As$ channel layer sandwiched between two heavily Si-doped n^+-type $Al_{0.225}Ga_{0.775}As$ layers. A small deviation of within ±7.6% in Lg is obtained with the 0.13-μm gate. All the devices are passivated using SiN film with a thickness of about 100nm.

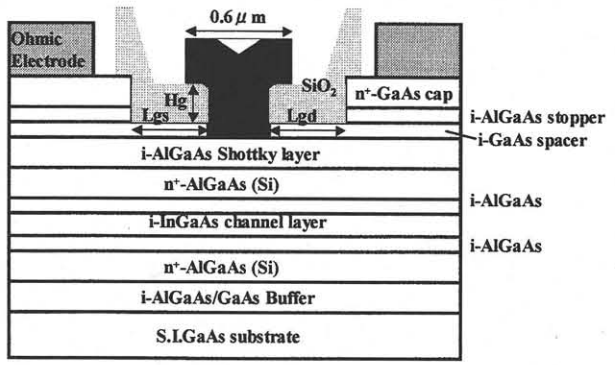

Fig.3 Schematic cross section of the device structure

3. Characteristics of Fabricated HJFETs

The characteristics of HJFETs were investigated as a function of the SiO_2 removal ratio along the gate-finger. A BHF etching time of 70s was selected to completely remove the SiO_2, considering an etching rate of 0.3μm/min around the gates.

Our fabricated standard HJFETs with Lg=0.13μm and Wg= 50μm×2 exhibited good DC characteristics with a maximum drain current (Imax) of 577mA/mm and a maximum transconductance of 376mS/mm. Only the gate-to-drain breakdown voltages were dependent on the removal ratio, i.e., 12.0V and 12.4V for 0% and 100%, respectively. The DC characteristics exhibited a small deviation of within ±3% at each removal ratio over the wafer.

Figure 4 shows the current gain cutoff frequency (f_T) and the extrapolated maximum frequency of oscillation (fmax) as a function of the SiO_2 removal ratio along the gate finger (DC bias: Vds=3.5V and Ids=Imax/2). Both values increase linearly as the removal ratio increases. Figure 5 shows the extracted values of the gate-to-source capacitance and intrinsic transconductance. The behaviors of f_T and fmax are well explained by the difference in the parasitic gate-to-source capacitance. For HJFETs with a SiO_2 removal ratio of 100%, a high f_T of 66.4GHz and an extrapolated fmax of 261GHz were obtained. RF characteristics also exhibited a small deviation of within ± 5% at each removal ratio over the wafer.

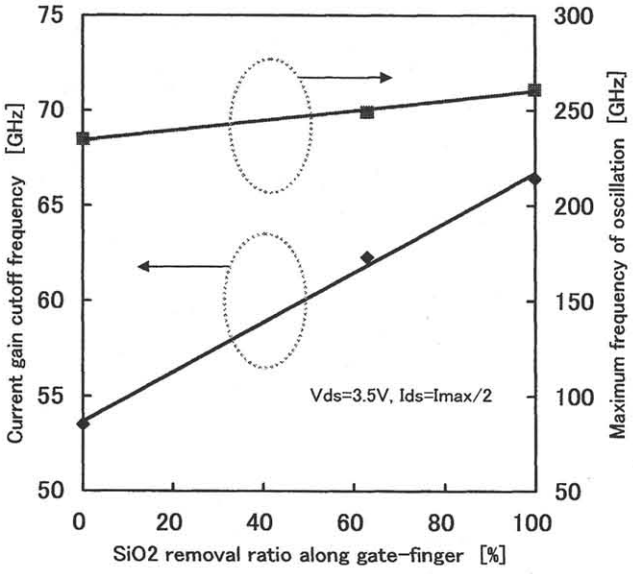

Fig.4 Current gain cutoff frequency and maximum frequency of oscillation

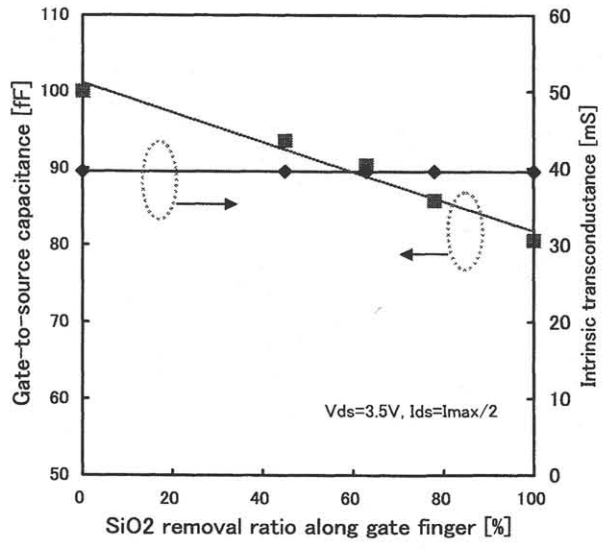

Fig.5 Gate-to-source capacitance behavior

The gate yield was estimated with an optical microscope for our standard HJFETs. Figure 6 shows the failure-ratio in the HJFET gate shape with the etching time of 70s as a function of the SiO_2 removal ratio. Gate shape failure is not observed in the removal ratio range from 0% to 60%. The etching causes significant failure when the removal ratio is over 60%, although the RF characteristics improve as the SiO_2 removal ratio increases. To secure high device yield, an SiO_2 removal ratio from 0% to 60% is suitable for a normal fabrication process. For the removal ratio of 60%, f_T and fmax are about 62GHz and 245GHz.

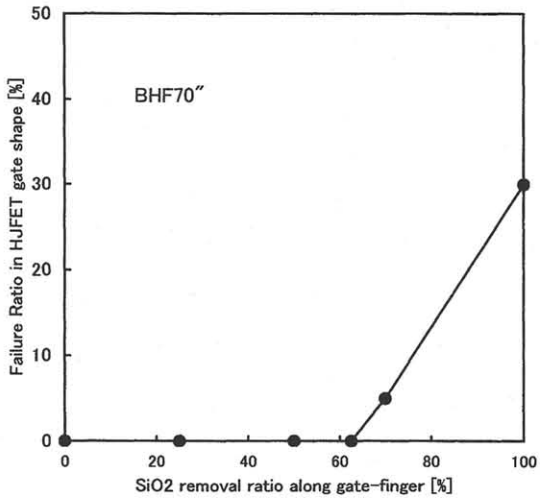

Fig.6 Deterioration ratio in HJFET gate shape

4. Conclusion

To meet the needs for both a high yield and high-frequency gain at the same time, we have developed a new gate fabrication technology, in which gates are partially supported along the fingers with SiO_2. The structure can be built using a fabrication process where the SiO_2 around the embedded gates is partially removed along the fingers in a striped pattern.

A gate shape failure is not observed when using a SiO_2 removal ratio from 0% to 60% and a BHF etching time of 70s. This range of ratios is suitable for a normal fabrication process. The HJFET with a removal ratio of 60% exhibited a high f_T of 62GHz and an fmax of 245GHz.

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