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Lateral *p-n* Junction in High Electron-Mobility Structure

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1 Introduction

The *p-n* junction is one of the bedrock structures in semiconductor technology, and its use in nanoscale devices is becoming of great interest. The exploitation of their electroluminescence properties opens up the possibility for nanoscale light sources. A high degree of control over the size of a *p-n* junction can be gained by a lateral arrangement. Lateral *p-n* junctions have been formed in GaAs molecular beam epitaxy by crystal plane dependent doping [1], and electroluminescence of these structures has been investigated by several groups, e.g. in [2, 3, 4], and spacially resolved in [5].

Here we propose an alternative way to produce nanoscale, lateral *p-n* junctions based on wet etching of a AlGaAs/GaAs structure. A simulation of the structure shows that a *p-n* junction can be formed in a high electron mobility region. In addition it allows arranging it with other electronic components with high accuracy, since the junction can be defined by electron beam lithography. The simulations were performed using the software package ATLAS from Silvaco.

2 Structure

The band structure of the system on which the device is based is shown in Figure 1. The detailed composition is shown in Figure 2 and 3. The GaAs/AlGaAs heterostructure contains two doped layers that provide carriers of opposite type for the undoped GaAs layer (region III), and partially compensate each other. The ratios of the two doping levels are chosen such that the majority carriers in region III are holes. If region I is removed, as shown in Figure 1(*b*), the majority carriers will be electrons and a *p-n* junction forms at the edge of the mesa. Figure 3 shows the carrier densities measured of region III across the junction. Since the simulator models a 2D structure many values are in units $1/\mu$m. In our case we assume a channel of width $1\,\mu$m to obtain values that can be compared to devices that this simulation aims to model.

3 Results and Conclusion

The modeling of the current-voltage curves at room temperature is shown in Figure 4. It shows the expected rectifying behavior of a *p-n* junction. The capacitance was modeled by applying a small AC voltage of 1.0 MHz, and the calculated capacitance for $V_B = 0\,\mathrm{V}$ is 60 aF. Increasing the backward bias voltage to $V_B = -2.0\,\mathrm{V}$ results in a capacitance of 40 aF. Figure 3 shows the current flow when a forward bias of $V_B = 1.2\,\mathrm{V}$ is applied. In the *n*-type region the current is confined to region III, whereas in the *p*-type region it can also penetrate into the *p*-doped layer. However, the recombination takes place in region III, and mostly within the *p*-type region. Here, bright areas show high recombination rates of electrons and holes. Finally, the diagram in Figure 5 shows the ratio of radiative recombination with respect to the total recombination integrated over the whole structure. The maximum efficiency of $\eta = 0.8$ is reached at a bias voltage of $V_B = 1.5\ V$. If the bias voltage is increased the recombination area spreads out and reaches the electrodes. The large number of impurities in this region causes the efficiency to drop as the voltage is further increased. This problem would not occur for a longer channel, i.e. wider spaced electrodes. At lower temperatures the recombination time will decrease and hence recombination will take place in a smaller region.

Fabrication of such a device can be achieved in a single step after the wafer has been grown using slow wet etching. A particular advantage would be that the *p*-type and *n*-type regions are side by side on the sample surface, therefore all the electric contacts can be made on the same side of the sample using coplanar geometry. Moreover, electrically insulating substrates can be used, simplifying electrical isolation of multiple devices made on the same substrate.

This paper will describe a simulation and experimental investigation on such devices.

References

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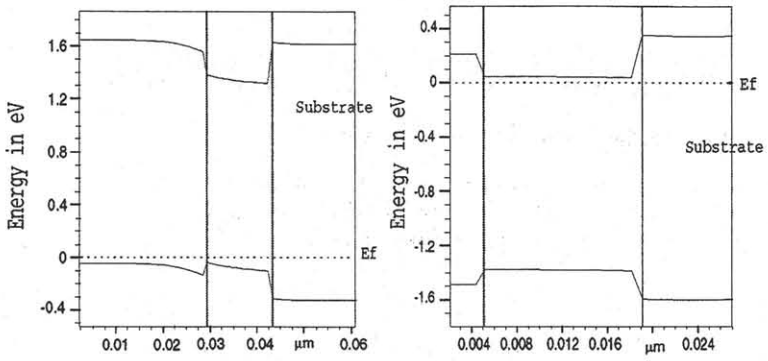

Figure 1: Band structure of the unetched part (left) and the etched part of the device (right), perpendicular to the surface at $V_B = 0\,\mathrm{V}$.

No	Depth in Å	Material	doping in cm^{-3}
I	240	$Al_{0.22}Ga_{0.78}As$	$N_a = 1.5 \times 10^{18}$
II	30	$Al_{0.22}Ga_{0.78}As$	$N_a = 1.5 \times 10^{14}$
III	140	GaAs	$N_a = 1.5 \times 10^{14}$
IV	30	$Al_{0.4}Ga_{0.6}As$	$N_a = 1.5 \times 10^{14}$
V	10	$Al_{0.4}Ga_{0.6}As$	$N_d = 1.0 \times 10^{18}$
VI	4000	$Al_{0.4}Ga_{0.6}As$	$N_a = 1.0 \times 10^{14}$

Figure 2: Materials and doping levels used for p-n junction simulation

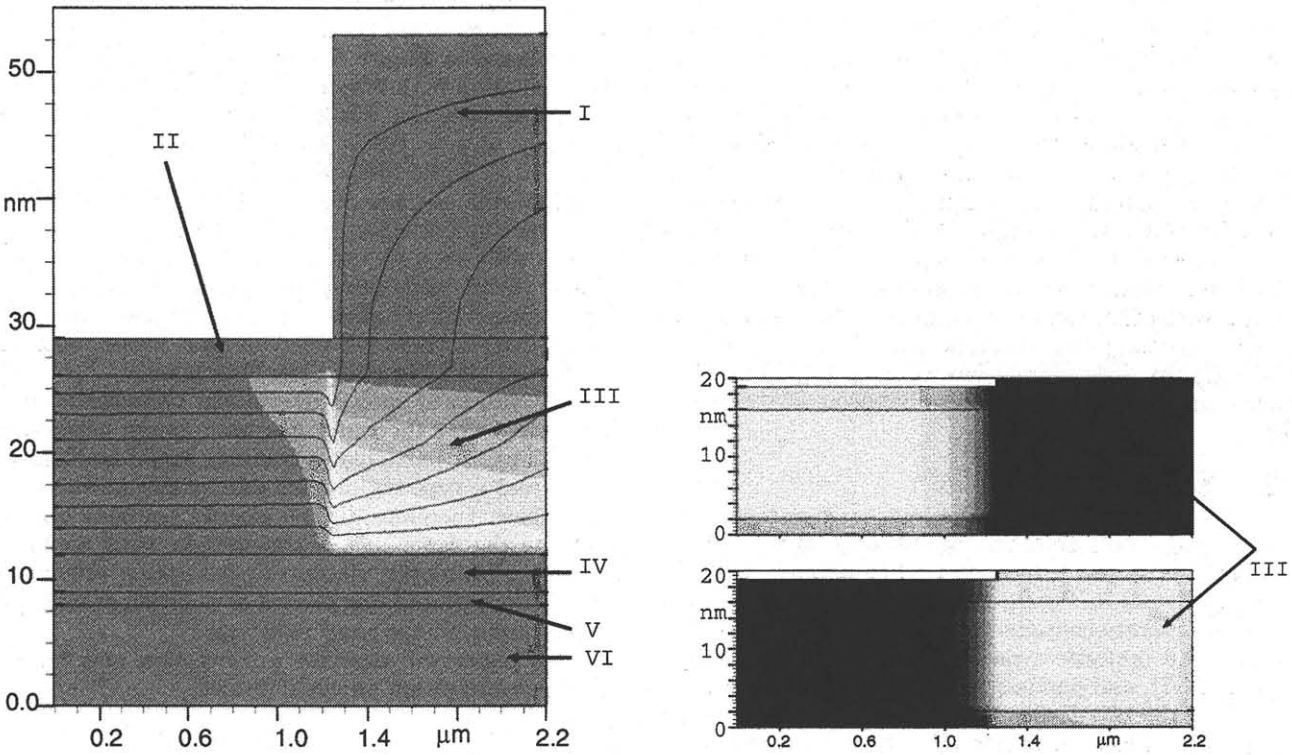

Figure 3: The left part shows the current flow lines and the recombination rate at $V_B = 1.2\,\mathrm{V}$. Light areas correspond to high recombination rates. Regions I - VI are defined in the Figure 2. The carrier distribution in region III is shown on the right (top: electrons, bottom: holes). Light areas correspond to larger values.

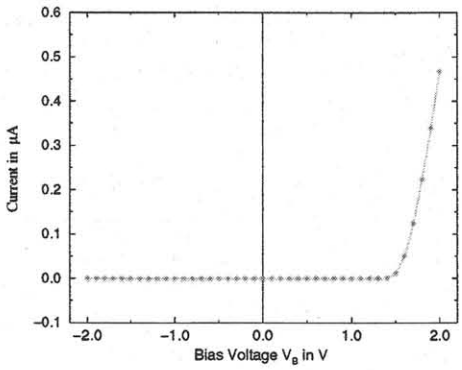

Figure 4: Rectifying behavior of p-n junction.

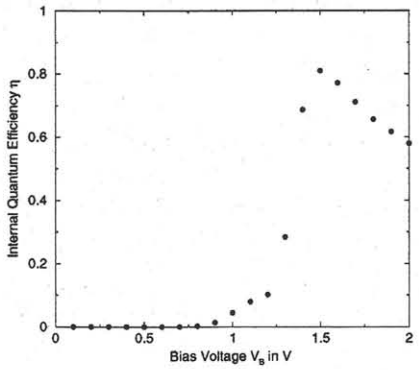

Figure 5: The variation of the efficiency of the simulated device with forward bias voltage.