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Carrier Transport of SiN Gate Dielectrics for Dual-Gate CMOSFETs

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1. Introduction

The scaling of gate oxide thickness below 2nm will face the problem of increase in the gate direct tunneling current. In general, the direct tunneling current is a strong function of physical thickness. Therefore, it is efficient to use the material with higher dielectric constant compared to SiO_2 as a gate insulator to reduce the direct tunneling current and to achieve the same equivalent oxide thickness (EOT). SiN is a promising material among several candidates due to the compatibility with the conventional CMOS process integration and higher dielectric constant compared to SiO_2. Although the characteristics of CMOSFET with SiN gate dielectric have been reported [1-2], the carrier transport of SiN gate dielectric has not been clarified yet, especially for pMOSFET with p+ poly-Si gate electrode.

In this work, we investigate the gate current of both pMOSFET and nMOSFET with SiN gate dielectric. We report that gate current reduction compared to SiO_2 is small for pMOSFET than that of nMOSFET. This asymmetric behavior is discussed in terms of carrier conduction mechanism and band diagram of SiN.

2. Experimental

We fabricated n- and pMOSFETs using conventional dual-gate CMOS process. The SiN films were deposited by LPCVD. Post deposition anneal was performed to reduce trap sites. The final physical thickness of SiN was 3.3nm. We also prepared thermal oxide samples with the physical thickness of about 2.15nm and 2.35nm as the reference. EOT was extracted at strong accumulation by C-V measurement. The EOT of 3.3nm-thick SiN was about the same as 2.35nm-thick SiO_2. Band diagram of SiN was measured by XPS analysis.

3. Results and discussion

Fig.1 shows the relationship between EOT and the gate current at electric field of 5 MV/cm biased in inversion. For nMOSFET, the gate current through SiN is reduced by about one order of magnitude compared to SiO_2 with the same EOT due to increase in physical thickness. However, the gate current through the SiN is the same as that through the SiO_2 for pMOSFET, which is contrary to the expectation of one order of magnitude reduction.

In order to clarify this asymmetric behavior of n- and p-MOSFETs, carrier conduction mechanism and band diagram is investigate in detail. Fig.2 shows the possible carrier conduction processes in the gate dielectric in an inverted pMOSFET. Possible processes are: (a) valence band hole tunneling from the Si Substrate, (b) valence band electron tunneling from the p+ poly-Si electrode, and (c) conduction band electron tunneling from the p+ poly-Si electrode [3]. In addition, (d) trap-assisted tunneling (Pool-Frenkel type) should be also considered for CVD SiN, which might have larger amount of traps than SiO_2. For nMOSFET, the carrier of the gate current is always inversion-layer electron, so that direct tunneling and trap-assisted tunneling of inversion electron should be considered as the possible mechanism of gate current.

Firstly, we measured the temperature dependence of the gate current to know whether the trap-assisted process is the case or not, since the trap-assisted tunneling shows strong temperature dependence while the direct tunneling current does not. It was found that the temperature dependence of SiN-MOSFET is the same as SiO_2-MOSFET for both pMOSFET and nMOSFET as shown in Fig.3. Small activation energies of ~30meV for all the cases confirm that the gate current is dominated by the direct tunneling from the gate and/or inverted Si substrate.

Secondly, in order to determine the dominant direct tunneling process, we performed the carrier separation measurement [3]. For both pMOSFET and nMOSFET, and regardless of either SiN or SiO_2, the gate current I_G is dominated by the source/drain current I_S+I_D as shown in Fig.4. This indicates that the carriers of the inversion layer tunnel to gate electrode for all cases.

Finally, in order to determine the energy band diagram of both SiN/Si and SiO_2/Si structures, we measured the energy loss spectra of O_{1s} and valence band spectra as shown in Fig.5. From these results, we estimated the energy gap and the valence band offset to Si substrate[4]. Considering the Si bandgap of 1.12eV, we can obtain the electron barrier height. Fig.6 shows the barrier height for both SiN/Si and SiO_2/Si structures. It is found that the electron barrier height in SiN/Si structure is lower by 0.3eV compared to that in SiO_2/Si structure, while the hole barrier height in SiN/Si structure is lower by 0.54eV than SiO_2/Si structure. Using the measured values of barrier height, the direct tunneling current for both n- and p-MOSFETs is estimated using WKB-approximation, as shown in Fig.7. The calculated tunneling current in SiN is reduced by about one order of magnitude compared to that in SiO_2 with the same EOT for nMOSFET, while that of SiN is the same as SiO_2 for pMOSFET, which is consistent with the measurement results shown in Fig.1. According to the above discussions, asymmetric behavior of gate current reduction in n- and p-MOSFETs by using SiN can be attributed to the asymmetric change of barrier height in conduction band and valence band.

4. Conclusions

The carrier conduction mechanism of both pMOSFET and nMOSFET with SiN gate dielectric was clarified. The temperature dependence of the gate current shows that the trap-assisted tunneling does not occur and the direct tunneling is dominant. From the carrier separation measurement, it was found that the carrier tunneling from the inversion layer is the dominant transport process. The results of XPS measurement shows that the electron barrier height in SiN/Si structure is lower by 0.3eV compared to that in SiO_2/Si structure, while the hole barrier height in SiN/Si structure is lower by 0.54eV than SiO_2/Si structure. The electron tunneling current in SiN is reduced compared to SiO_2 due to the increase of the physical thickness. On the other hand, the hole tunneling current in SiN is almost the same as that in SiO_2 due to the significant lowering of barrier height in valence band side of SiN compared to that of SiO_2.

References : [1]H.-H.Tseng, et al., IEDM Tech. Dig. p.647 1997. [2]X. Qiang, et al., IEDM Tech. Dig. p.860, 2000. [3] Y. Shi, et al., IEEE Trans. Electron Device, **45**, p.2335, 1998. [4]H. Itokawa, et al.,Extended Abstracts of SSDM, p.158, 1999.

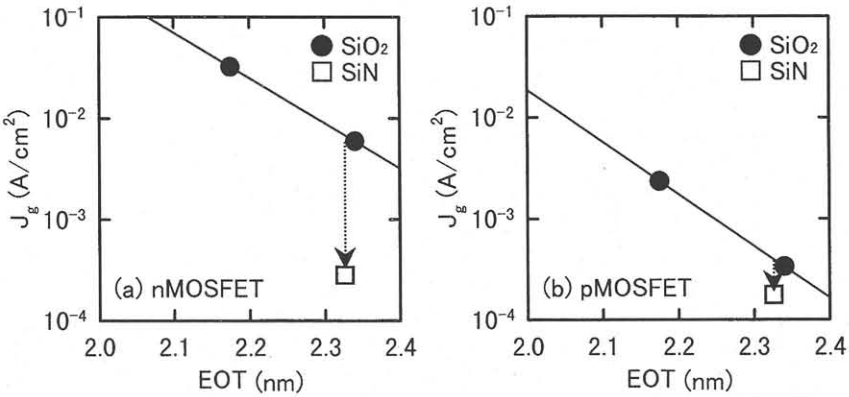


Fig.1 The relationship between EOT and the gate current of (a)nMOSFET and (b) pMOSFET.

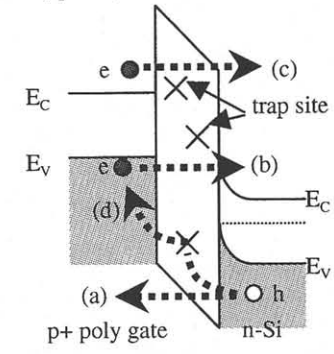


Fig.2 The possible conduction processes in pMOSFET.

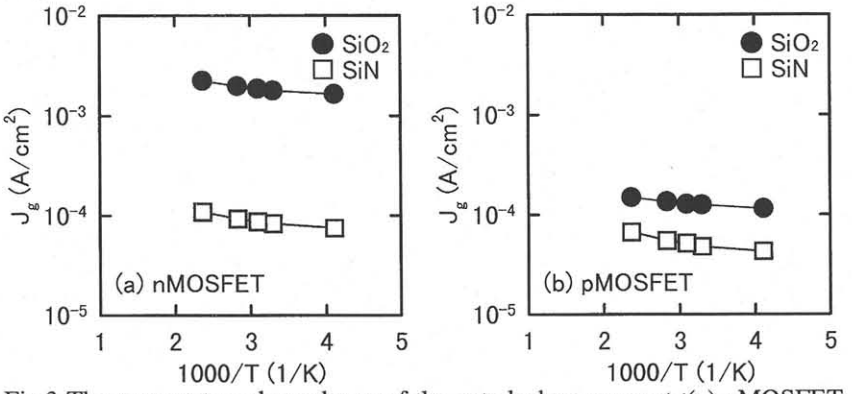
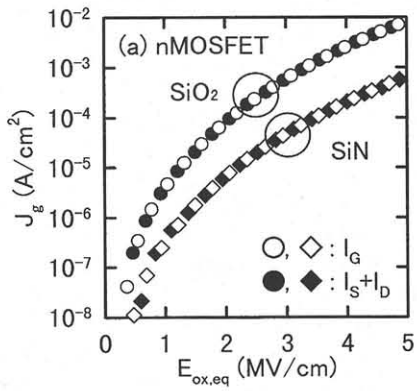


Fig.3 The temperature dependence of the gate leakage current. (a) nMOSFET and (b) pMOSFET.



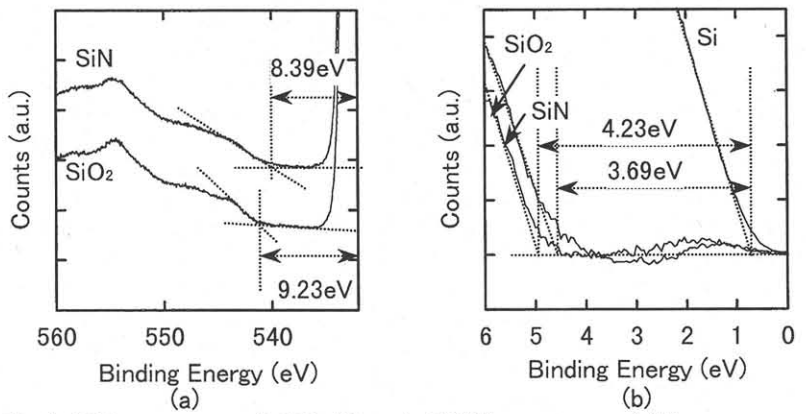


Fig.5 XPS spectrum of SiO_2/Si and SiN/Si structures. (a)Energy loss spectrum of O1s. (b) Valence band spectrum.

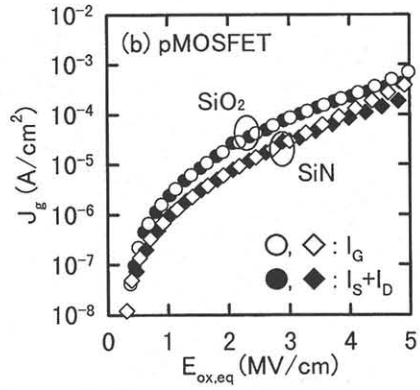


Fig.4 Carrier separation results of (a)nMOSFET and (b)pMOSFET.

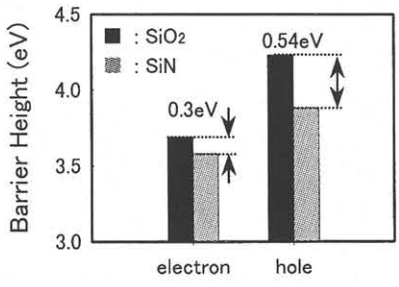


Fig.6 The barrier height of electron and hole.

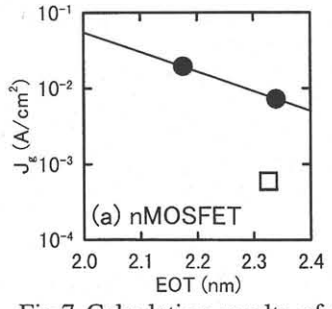


Fig.7 Calculation results of the direct tunneling. (a) nMOSFET and (b) pMOSFET.