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Saturation Phenomenon of Stress Induced Gate Leakage Current

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1. Introduction

SILC (Stress Induced Leakage Current) is one of the serious issues for the gate oxide reliability and many reports are published [1]. DiMaria et. al presented the saturation phenomena of SILC degradation[2,3]. Percolation theory is one of the useful models for explaining an increase of the gate leakage current due to SILC, but cannot explain the saturation phenomena of degradation. In this paper, we measured the features of the SILC saturation, comparing with the degradation of the Vg-Id and charge pumping characteristics. Moreover, the physical image for degradation by the SILC is proposed.

2. Saturation of SILC degradation

The gate current is increased with increasing the stress at constant voltage as shown in figure 1. This increase is explained by a generation of the defects in the oxide according to the percolation theory as shown in figure 2.

The degradation of stress induced leakage current is represented by the shift of the gate voltage, "ΔVg", with keeping Ig=0.1nA as shown in figure 1(b). In figure 3, ΔVg is increased rapidly at first stage until 10s, where log(ΔVg) is proportional to log(time). This is result of increase with the leakage paths in gate oxide. However, after 10s, saturation of ΔVg can be clearly observed, where the ΔVg is proportional to log(time) as shown in figure 3(a).

Saturation of the voltage shift by SILC can be developed as shown in figure 4. Both $y=ax^b$ and y=b+log(x) are used to fit time-ΔVg characteristics of time<10s and time>10s respectively. Two fitting lines are touched at the point of ΔVg=300mV. This point means the start of saturation of the SILC degradation and we express this voltage shift to be "ΔVg,sat".

3. Features of ΔVg,sat

Degradations by SILC with various stress voltage are plotted in figure 5. ΔVg,sat is given by the filled symbols in this figure. It can be observed that ΔVg,sat is kept constant against the stress voltage.

Figure 6 shows a dependence of ΔVg,sat on the gate oxide thickness. The ΔVg,sat is linearly increased to the thickness of gate oxide. Moreover, it notes that oxides fabricated different processes show different ΔVg,.

Moreover, temperature dependence of ΔVg,sat is presented in figure 7. SILC degradation becomes severe when stress temperature is high (figure 7a). However, the time dependences of ΔVg cannot be observed with various temperatures. Universal curve can be seen, normalizing the time to 27C data. This means that no dependence on temperature can be seen for ΔVg,sat as shown in figure 7b.

4. Degradation of threshold voltage and CP current

It is considered that degradation is caused by injected hole from the gate electrode [4]. In figure 8, SILC degradation is plotted as a function of the injected hole deduced from substrate current. Increase of the threshold voltage is also plotted in the same figure by monitoring the Vg-Id characteristics. In the region of ΔVg>300mV, the degradation of the threshold voltage is rapidly increased even if the shift of the gate voltage is saturated. Moreover, it is found that charge pumping current is increased in this region as shown in figure 9. Charged defects increase the SILC and the threshold voltage. However, interface states have no influence on the SILC. In this result, the hole is continuously injected in the gate oxide after saturation of SILC and makes the interface states.

5. Model of SILC saturation

Injected hole makes the defects in the gate oxide (A1=>A2=>A3 in figure 10) and the interface states (B1=>B2=>B3 in figure 10). First, the hole makes the defects in the oxide as shown in figure 11(a). In this stage, seeds of the defects (for example the oxygen vacancy) are defined by the quality of the gate oxide and hole just helps for making defects. Therefore, finally, the SILC is saturated even if the hole is continuously injected into the gate oxide (figure 11 b). It notes that the maximum quantity of defects is decided by the oxide quality. Hole doesn't create new seeds of defects. After saturating the defects, hole works to make the interface states and increase the threshold voltage continuously (figure 11 c). This model also explains no dependence on the saturation of SILC when the hole energy and quantity are increased. Moreover, it can be clearly understood that gate oxides fabricated by different processes have different ΔVg,sat.

6. Conclusion

Saturation of the SILC is measured with various stress voltage, oxide thickness and stress temperature, comparing with the threshold voltage and charge pumping current. It is found that the maximum quantity of defects is decided by the oxide quality. Hole doesn't create new seeds of defects but just helps activating the defects.

7. Acknowledge

Authors would like to thank to Dr. Kamakura in Osaka University for their helpful and kind discussion.

References

[1] R. Degraeve et. al, IEEE trans. Electron Devices, vol.45 ,1998, p.904
[2] D.J. DiMaria et. al, J. Appl. Phys., vol.89, 2001 , p.5015
[3] J. Sune et. al,, Abst. in SISC, 1999
[4] K.F.Schuegraf et. al, J. Appl. Pyhs.. vol.76, 1994, p3695

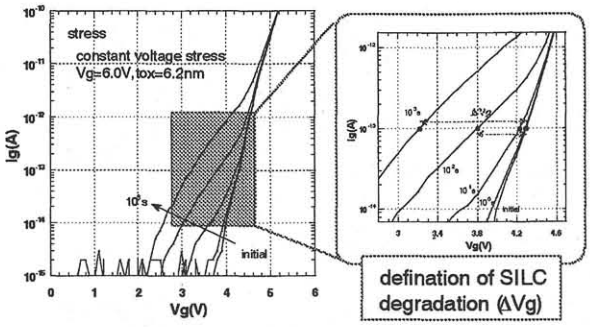


fig.1: Increase of gate current as time of constant voltage stress is increased

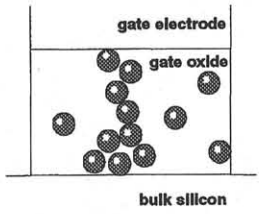


fig.2: Schematic image of SILC (Stress Induced Leakage Current) based on parcoration theory.

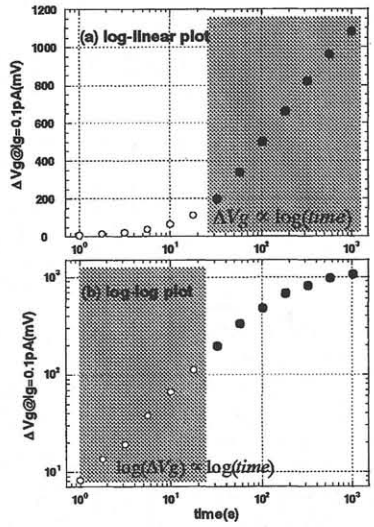
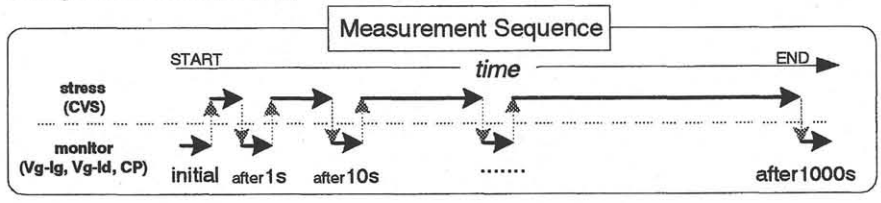


fig.3: Degradation of ΔVg @Ig= 0.1pA as a function of time.



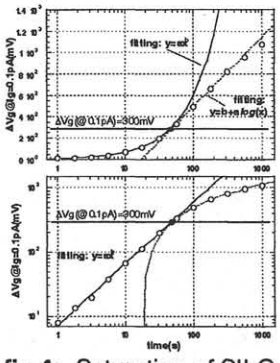


fig.4: Saturation of SILC degradation deduced by y=axb and y=b+alog(x).

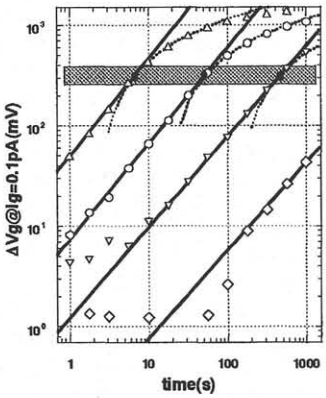


fig.5: Voltage degradation of SILC saturation with various voltage stress.

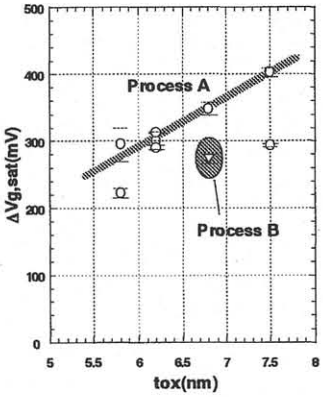


fig.6: Voltage degradation of SILC saturation with various gate oxide thickness.

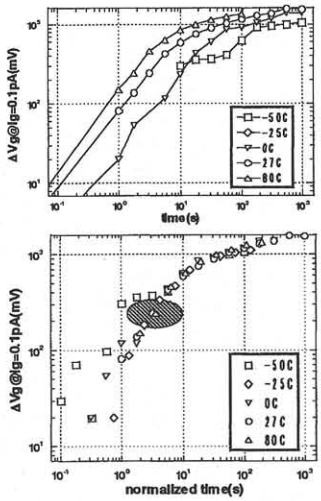


fig.7: Voltage degradation of SILC saturation with various temperature.

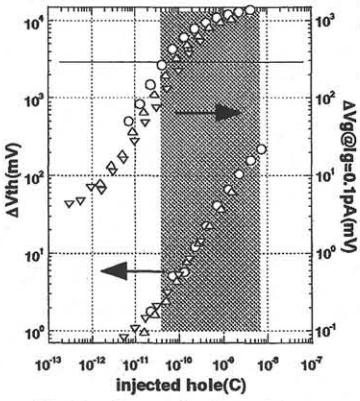


fig.8: Degradation of the threshold voltage.

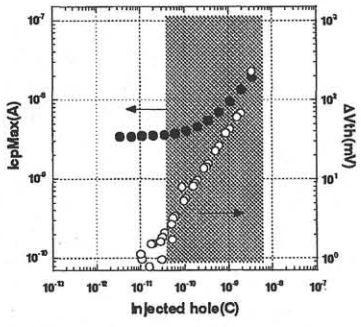


fig.9: Degradation of the charge pumping current.

fig.10: Schematic Image of making defects(A1=>3) and interface states (B1 =>3).

$$Si - H + 2h^{+} \leftrightarrow 2Si^{\cdot} + H_2$$

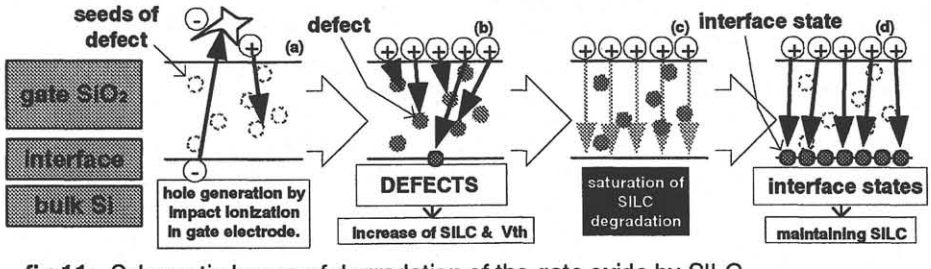


fig.11: Schematic Image of degradation of the gate oxide by SILC.