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Monitoring Degradation of Source/Drain Extension in Sub-Quarter-Micron MOSFET's

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1. Introduction

The interface traps in high doping drain extension (DE) region deteriorates the characteristics of quarter and sub-quarter-micron MOSFET's in several ways such as increasing series resistance, cutoff leakage current, etc. However, traditional methods, such as charge pumping and C-V, are not effective in measuring the interface traps in this region. Originating from the newly developed Direct-Current Current-Voltage (DCIV) technique [1], a novel approach is demonstrated to fill this gap.

2. Analysis and Simulation

p-MOSFET's are taken as examples for analysis. In quarter-micron and sub-quarter-micron p-MOSFET's where source/drain extension doping concentration is very high and gate oxide is very thin, when raising the gate-drain voltage V_{gd}, the electric field under the gate-drain overlap becomes very strong and electron tunneling in band gap may occur. If the drain-bulk pn junction is reverse biased, the tunneling current is referred as Gate-Induced-Drain-Leakage (GIDL) [2-4]. If the junction is forward biased such as in the DCIV measurement, band-to-band tunneling is forbidden and only two-step process, namely, electron captured from conduction band to an interface trap, and subsequently tunneling from the trap to the valence band (TTT) takes place [4] (Fig. 1.). The net thermal capture rate from the conduction band to the trap is [5]:

$$NTC_e = C_n[n_1 f_t - n_s(1 - f_t)], \qquad (1)$$

where C_n is the electron capture rate, $n_1=n_i e^{(E_t-E_i)/kT}$, f_t is the electron occupation factor at interface trap energy E_t, and n_s is the conduction electron concentration at Si surface. The net tunneling rate from the trap to the valence band is [6]:

$$NT_h = \frac{f_t - f_v}{\tau_h}, \qquad (2)$$

where f_v is the electron occupation factor in the valence band and τ_h is the hole tunneling time constant [4].

In the steady state, $NTC_e = NT_h$. By simple algebra from Eqs.1 and 2 and neglecting the small term n_1, we can obtain:

$$NT_h(E_t) = \frac{(1 - f_v(E_t))\, n_s}{C_n^{-1} + n_s \tau_h(E_t)}. \qquad (3)$$

Fig.2 (a) shows the simulation results of Eq.3, using the τ_h formula and parameters in [4]. With DE doping concentration 2 x 10^{19} cm^{-3}, interface traps at certain energy level $E_{teff} \approx E_v + 0.43$eV are most effective and dominate the tunneling and there is a peak of tunneling rate under certain surface potential (0.48 V).

As a comparison, the Shockley-Read-Hall (SRH) thermal recombination rate through the interface traps [7] is also simulated for the same conditions. It shows that the SRH current is two orders of magnitude lower than that of the TTT current. So the SRH current can be neglected.

Considering the fact that only interface traps at E_{teff} play a dominant role in tunneling, we can roughly estimate the tunneling current I_T by

$$I_T = N_{it}\,[q\, NT_h(E_{teff})]\, W, \qquad (4)$$

where W is the channel width , N_{it} is the equivalent effective number of interface traps per unit channel width in the DE region. From Fig. 2 (a), $NT_h(E_{teff}) \approx 6\times10^5$ /s, or one interface trap will induce 0.1pA current. This is extremely sensitive.

3. Results and Discussion

0.25-μm and 0.18-μm technologies, n-and p-MOSFET's with different channel width/length and oxide thickness were investigated. Fig.3 shows three bulk current peaks under the channel hot carrier (CHC) stresses for 0.25 μm technology p-MOSFET. The first two peaks constitute the DCIV spectra where peak BC measures the interface traps in the base-channel region, and peak JSC measures the interface traps in the drain junction space charge region [7,8]. The third and new peak DE corresponds to the TTT current, which measures the interface traps at the gate overlapped DE region. The measured peak magnitude and peak gate voltage are consistent with the simulation. The peak position shifts to higher V_{gd}, under stress, implying a negative charge trapped in the oxide.

Fig.4 shows the similar results however under constant current FN stress. It is shown that the inversion FN stress is more effective than the accumulation FN stress in generating interface traps, at both BC and DE regions, when the stress current is the same. Fig. 5 shows FN stress results for n-MOSFET. The DE bulk current doses not show a peak .We ascribe this to the higher doing concentration (1x 10^{20} cm^{-3}) in DE region of the n-MOSFET's. According to the simulation, the tunneling rate is higher, however the peak gate voltage is also higher and is out of the measurable range before the oxide breakdown.

Fig.6 shows the FN stress results for the 0.18 μm technology MOSFET's. In all the measurements, the gate currents were also monitored. In the sweeping range of V_{dg} in Fig.6, the gate current is negligible compared to the bulk current I_b and therefore I_b is mainly contributed by the TTT process.

4. Conclusion

Stress induced degradation at gate overlapped high doping DE region in MOSFET's was characterized by measuring forward biased bulk current at high gate voltage. The current is demonstrated originating from thermal-tunneling via interface traps from the conduction band to the valence band. Simulation based on this model predicts a huge peak at high gate voltage and is quantitatively in good agreement with the measurements.

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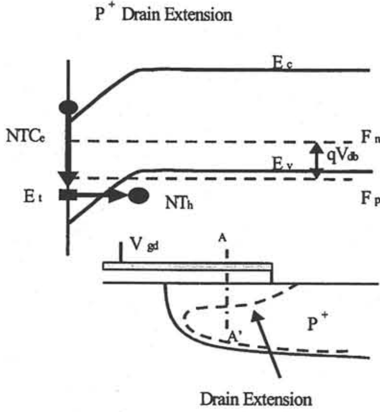
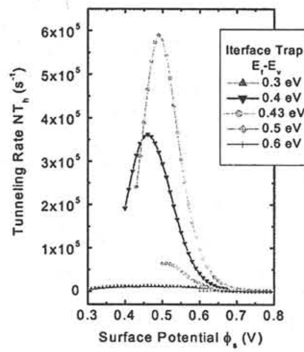


Fig. 1. p-MOSFET drain extension band bending under positive gate-drain voltage. Drain-bulk p-n junction is forward biased. Electrons are captured by interface trap E_t from the conduction band and then tunneling to valence band.



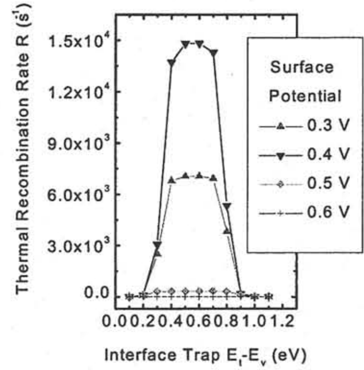


Fig. 2. (a) Simulation results of NT_h (E_t) by Eq. 3 against the surface potential Φ_s when the forward biased voltage V_{db}=0.4 V. (b) Simulated Shockley-Read-Hall (SRH) thermal recombination rate through interface traps. DE doping concentration is 2 x 10^{19} cm^{-3} . Thermal capture rate C_n = 2.3 x 10^{-8} s/cm^3 [1].

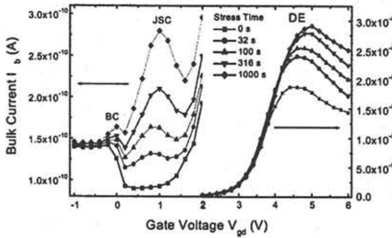
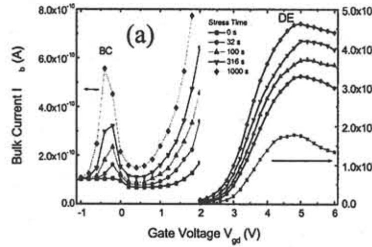


Fig.3. I_b versus V_{gd} before and after channel hot carrier (CHC) stresses. Three peaks (BC, JSC and DE) are observed, corresponding to the interface traps at Base Channel, Junction Space Charge, and Drain Extension regions respectively. Measurements were implemented at V_{db}= 0.4 V, V_{sub} =V_{bulk}= 0 V, while source was floated. CHC stresses were implemented by grounding source and bulk, while V_{gs}=-2V, and V_{ds}=-7V. 0.25 µm p-MOSFET. W/L=50/0.5 µm, T_{ox}=58Å.



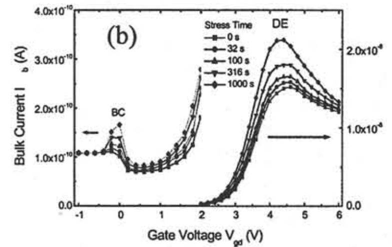


Fig.4. I_b versus V_{gd} before and after FN stresses. Measurement condition and devices are the same as in Fig. 3. FN stresses were implemented by grounding source, drain, and bulk, while (a) I_g=-3nA (negative V_g), (b) Ig=+3nA (positive V_g).

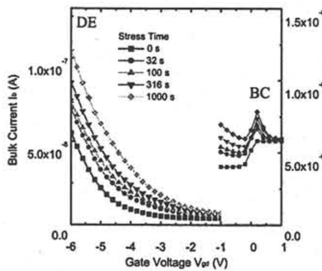
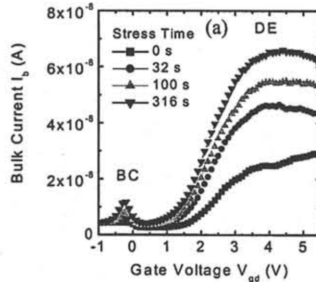


Fig.5. I_b versus V_{gd} before and after FN stresses (I_g=+5nA, positive V_g , V_d=V_b=V_s=0V). Measurements were implemented at V_{db}= 0.5 V, V_{sub} =V_{bulk}=0 V, while source was floated. 0.25 µm n-MOSFET. W/L=50/0.5 µm, T_{ox}=58Å.



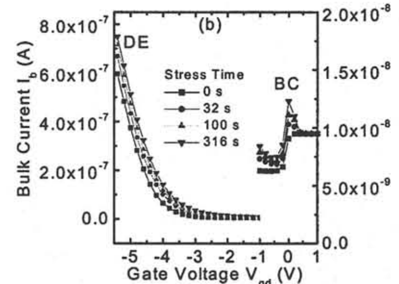


Fig.6. I_b versus V_{gd} before and after FN stresses. W/L=50/0.5 µm, T_{ox}=37Å. Measurements were implemented at V_{db}= 0.5 V, V_{sub} =V_{bulk}=0 V, while source was floated. FN stresses were implemented by grounding source, drain, and bulk, while (a) I_g=-6nA (negative V_g) for 0.18 µm p-MOSFET. (b) I_g=+100nA (positive V_g) for 0.18 µm n-MOSFET.