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Impact of Two-Dimensional Structure of nMOSFETs on Direct Tunnel Gate Current

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1. Introduction

The direct tunneling (DT) gate current (J_G) is one of the most important concerns for aggressively shrinking MOSFETs. Much effort has been paid to explain measured J_G-V_G curves under 1-D condition. However, they are theoretically insufficient, especially for low V_G. Moreover, there have been few studies to understand the behavior of DT in realistic structures of scaled MOSFETs. In this work, we have implemented new models for DT including band-gap narrowing (BGN) and incomplete impurity ionization (ICII) phenomena [1] into our in-house device simulator. It is found that BGN and ICII as well as DT are indispensable to reproduce the measured J_G-V_G curve including a low V_G region in the device simulation. The understanding of these phenomena is critically important to design the stand-by power dissipation of scaled MOSFETs. Moreover, it is clearly shown that 2-D structure of scaled MOSFETs affects J_G under low V_G condition.

2. Present approach

J_G is sensitive to BGN, which modulates the effective barrier height. The BGN is a function of carrier and ionized impurity concentrations as well as impurity concentration [1]. The impurity ionization rate depends on the carrier densities, which is modulated by J_G. Fig. 1 schemes a self-consistent calculation of BGN, ICII and J_G in the present device simulator. BGN is fed back to the drift term of the current density equation and the ICII to the Poisson equation. J_G is incorporated in generation-recombination term of the current continuity equation.

3. Gate current of long channel nMOSFET

Fig. 2 shows the distribution of the amount of BGN along the depth direction at the center of the channel. At the bottom of the gate n^+poly-Si, BGN decreases with V_G. This is because the electron concentration, which modulates the carrier-carrier and carrier-ion interactions, decreases with an increase in V_G. On the other hand, the amount of BGN at the substrate surface increases with V_G. This is due to the increase of the inversion electron concentration. Fig. 3 shows the distribution of the incomplete ionization rate under the same conditions as Fig. 2. Reasonable results, reflecting the electron concentration, are obtained. Fig. 4 shows measured [2] and simulated J_G-V_G curves in a long channel nMOSFET. In a sample with gate oxides of 2.1nm, a good agreement has been obtained in both gate polarities including the low V_G region. On the other hand, in a sample with gate oxides of 3.4nm, numerical noise level is higher than J_G under the condition.

4.Dependence of gate current on gate length

Fig. 5 shows the distribution of electron current density vector around a drain-side gate edge. It is observed that the current density is concentrated under the gate edge. This is because the electric field is concentrated at the gate edge. In order to investigate an effect of the concentration on J_G, the gate length (L_G) dependence of J_G –V_G curve is shown in Fig. 6. In a low V_G region, J_G is not scaled. Namely, the stand-by power dissipation is not scaled, since J_G around the gate edge becomes dominant as L_G is scaled down. The drain bias (V_D) dependence of J_G is also shown in Fig. 7. For higher V_G, J_G decreases exponentially with V_D. This is because the electric field around the drain-side gate edge decreases. On the contrary, when V_G is zero, J_G increases linearly with V_D, and the gate current polarity (+) is opposite. It is clearly shown that DT between the gate edge and the drain takes a significant role in the stand-by power dissipation.

5. Conclusion

The new models for DT, BGN and ICII were self-consistently implemented in the device simulator. It was confirmed that the measured J_G-V_G curves were successfully reproduced particularly in low V_G region. The impact of 2-D structure of MOSFETs on J_G was clearly shown from the viewpoint of the stand-by power dissipation in the present device simulation.

Acknowledgements

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References

[1] H. Watanabe and S. Takagi, to be published in J. Appl. Phys.

[2] S. Takagi, M. Takayanagi, and A. Toriumi, IEDM99-461.

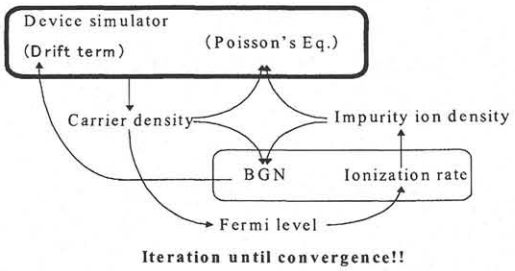

Fig. 1 A method to self-consistently calculate local BGNs, local impurity ionization rates and J_G in a device simulator..

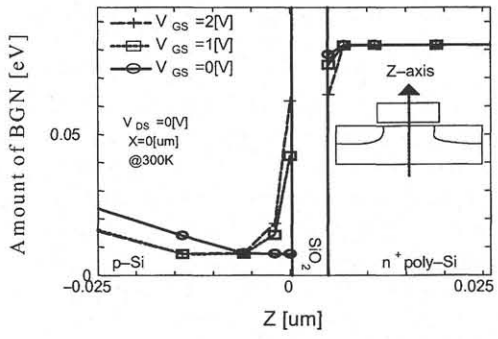

Fig. 2 Local BGNs along Z-axis at the center of the channel.

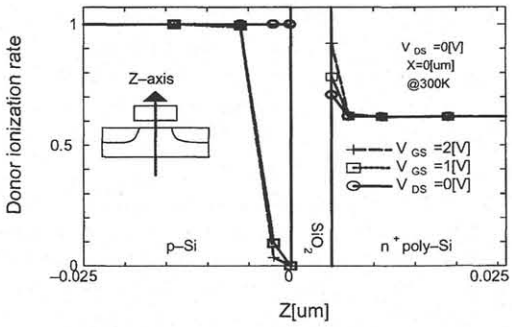

Fig. 3 Impurity ionization rate along Z-axis at the center of the channel.

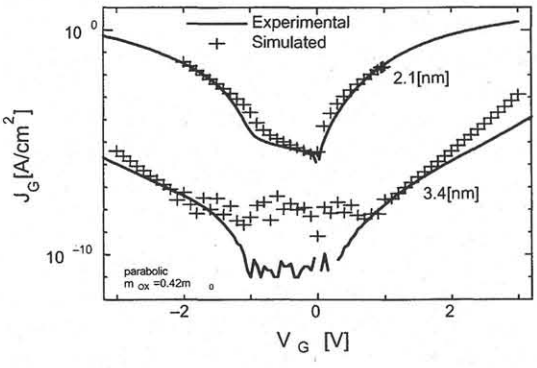

Fig. 4 Fitting between simulated and experimental J_G-V_G curves. In upper curve, t_{OX}=2.1[nm], N_{sub}=1.5E16[cm^{-3}], and N_{poly}=3E20[cm^{-3}]. In the other, t_{OX}=3.4[nm], N_{sub}=4E15[cm^{-3}], N_{poly}=3E20[cm^{-3}].

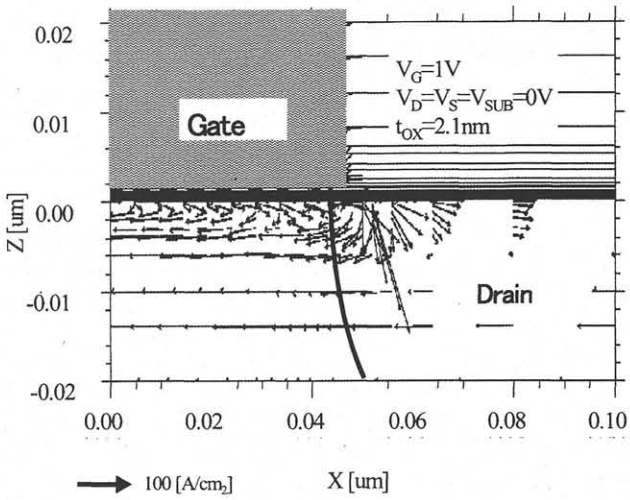

Fig. 5 Electron current vector near the drain edge.

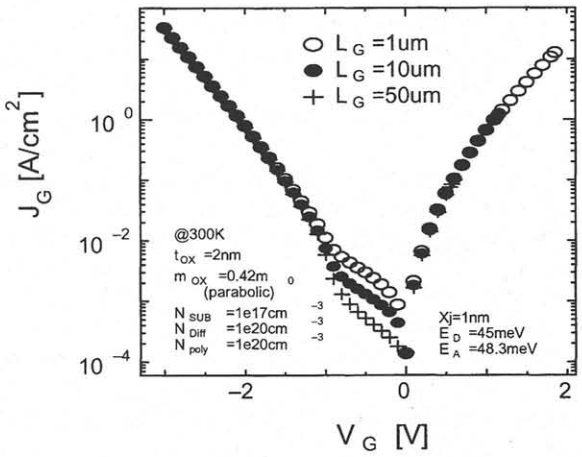

Fig. 6 L_G dependence of the simulated J_G-V_G curve.

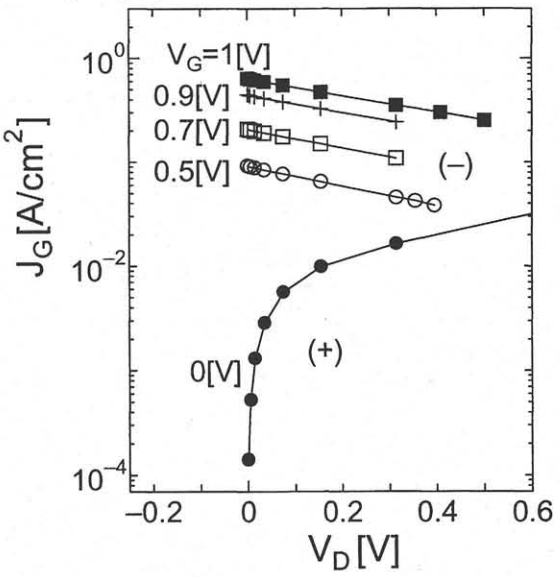

Fig. 7 Simulated J_G-V_D curve.