Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, Tokyo, 2001, pp. 146–147

F-2-1 (Invited)

# Sub-50 nm Local Channel MOSFETs by SALVO Process

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## Introduction

For future ULSI CMOS fabrication, it will be of cost and implementation advantages if the process is compatible with existing materials and tools. Moreover, device performances, $I_{on}$, $I_{off}$ and SCE, also need to be scaled along with a viable contact scheme of low $R_c$ and $R_s$ for gate and S/D. To achieve all those objectives, we first proposed the Self-Aligned Local-channel V-gate with Optical lithography (SALVO) process in a simulation study for high performance 25 nm PMOS [1]. Later, we present a SALVO CMOS process and first device data [2] with the following features: (1) self-aligned local channel (LC) implants to help produce abrupt lateral channel doping profiles for SCE suppression [3]; (2) sub-50 nm devices using only current production tools, including DUV lithography; (3) replacement gate [4][5] with low-$V_T$ dual-polysilicon for future $V_{DD}$ scaling (≤1.0 V). In this work, by the use of simulations we further explore the compatibility of SALVO process with dual-metal gate and high-k gate dielectrics for high performance sub-50 nm devices.

## SALVO Process Device Fabrication

Key stages of SALVO process flow for sub-50 nm MOSFETs are shown in Fig. 1. After STI and tub implants, the nitride/pad oxide sacrificial gates are patterned (Fig. 1a). After S/D implants, RTA, silicide, CMP gate planarization (Fig 1b) and wet removal of nitride, another thin nitride is deposited and etched back (stopping on pad oxide in order to maintain pristine underlying Si surface for channel carrier mobility and gate dielectric) to create inner spacers for local channel implants (Fig. 1c). For the replacement gate stack, since S/D formation is already performed, a variety of options can be explored: silicon oxide, nitrided oxide or high k for gate dielectric; polysilicon, poly-SiGe or metal for gate conductor. In fact, double-replacement can be readily performed to produce dual-metal gates (Fig. 1d). Note that the final gate length (Lg) is reduced by the inner spacers, producing sub-50 nm gates despite much larger sacrificial gate length. Moreover, the inner spacer width is really defined by the deposition of nitride and hence insensitive to RIE and trench opening (Fig. 2 insert). A 35% spacer-to-trench limit is chosen to ensure proper nitride step coverage. Even with the limit, a 25 nm final gate can be achieved, shown in Fig. 2, using just DUV lithography (193 nm ArF and phase shift). The first devices of SALVO NMOS and PMOS were fabricated using TiN/dual-polysilicon gates [2]. PMOSFETs especially show promises of practical future applications, including low $V_T$, low $V_T$ roll-off, good $I_{on}/I_{off}$ ratio and excellent sub-threshold slopes (S). Minimum Lg of 40 nm and 60 nm were obtained with S/D implant of 0.5 keV and 1keV B implanted S/D, respectively (Fig 4a and 4b).

## Simulation Study of Dual-Gate SALVO

The reason for such well-behaved ultra-short PMOS is SCE suppression by the lateral abruptness of channel doping, which is due to the fact laterally, the slope of the S/D and LC doping profiles are in opposite directions, causing the net profile to be sharper than either components (Fig. 5) [1]. In contrast, in the vertical direction the junction abruptness is controlled by the S/D alone. Using PROPHET process and PADRE device simulators [6], we find the sharpening of the lateral junction improves the $I_{on}/I_{off}$ tradeoff by >20% and reduces junction capacitance ($C_j$) by 17%, compared to the traditional design of uniform channel (UC) doping [2]. However, simulations for NMOS show that LC doping by boron is not effective in sharpening the lateral S/D to channel junction, due to the high diffusivity of boron in the electric field produced by the abrupt As junction [2]. It is likely that NMOS LC with lower-diffusivity dopant, such as indium, will be advantageous over UC. However, the shallow (15 keV) As S/D doping alone is sufficiently abrupt (4 – 5 nm /decade) to produce good SCE down to 40 nm [7]. For n+ polysilicon gate NMOS, the LC and UC with B or $BF_2$ produce comparable results [2]. While dual-polysilicon SALVO process had been demonstrated [2], in order to realize the high-performance scaling of SALVO, high k gate dielectric and dual-metal gate conductor are needed. The absence of polysilicon eliminates the gate depletion effect, and high k dielectrics produce thinner equivalent gate oxide thickness. The combination allows an equivalent electrical gate oxide thickness of 1.5 nm or below. For PMOS, metal such as Ni or $WN_x$ with a workfunction ($\Psi$) about 5.0 – 5.1 eV is chosen. Other parameters in the simulation study are 1.5 nm electrical $T_{ox}$, 1.0 V $V_{DD}$, varying As LC implant dose ($\Gamma$) and LC activation with spike anneal. With a slight tradeoff of $V_T$ roll-off (~5 mV/nm), ultra high $I_{on}$ can be achieved for sub-50 nm PMOS with good sub-threshold slopes (Fig. 6a, 6b and 6c). Using only drift-diffusion model and ignoring possible ballistic enhancement, we can obtain intrinsic PMOS $I_{on}$ of 750 μA/μm at ~160 nA/μm $I_{off}$ and S ≤ 95 mV/decade. For NMOS, metal such as Ta or $TaN_x$ with a $\Psi$ < 4.3 eV is chosen. Both LC and UC are simulated, with parameters of 1.5 nm electrical $T_{ox}$, 1.0 V $V_{DD}$ and varying $BF_2$ channel implant dose ($\Gamma$). UC produces the best results in terms of $V_T$ roll-off (~6 mV/nm) and $I_{on}$ (Fig. 7a, 7b and 7c). The combination of workfunction of 4.25 eV and UC of 5e12 $cm^{-2}$ produces 920 μA/μm intrinsic $I_{on}$ at ~160 nA/μm $I_{off}$, and S < 92 mV/decade. These numbers compare favorably with ITRS 2000 Roadmap Update: 350 μA/μm (P) and 750 μA/μm (N) at 160 nA/μm $I_{off}$ for high-performance 35 nm ASIC CMOS.

## Conclusion

Because of its great flexibility in materials and device tuning, SALVO introduces many new possibilities in CMOS scaling. Dual-metal gate SALVO can produce high performance devices in terms of drive current, SCE and sub-threshold slopes. Hence, SALVO provides a platform to fabricate and study ultra-short devices, using existing optical lithography.

## References

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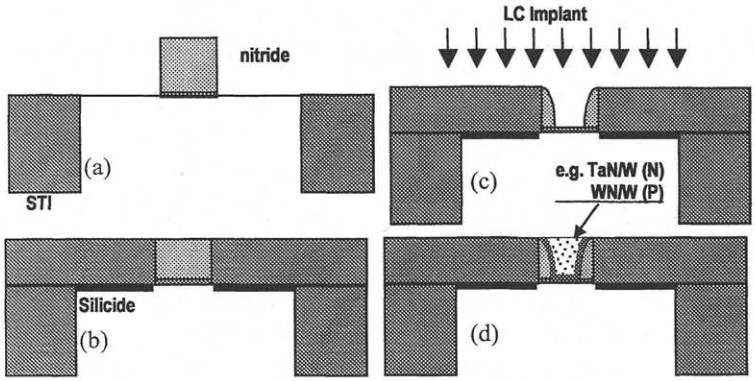


Fig.1: SALVO process for sub-50 nm gates: (a) STI and nitride/oxide gate (DUV phase shift); (b) CMP planarization after S/D formation and silicide; (c) nitride removal and 20 - 40 nm inner spacers producing <50 nm trench for local channel implants; (d) gate dielectrics and options: CMP metal gate (shown), or a-Si with n+/p+ gate doping and metal (not shown).

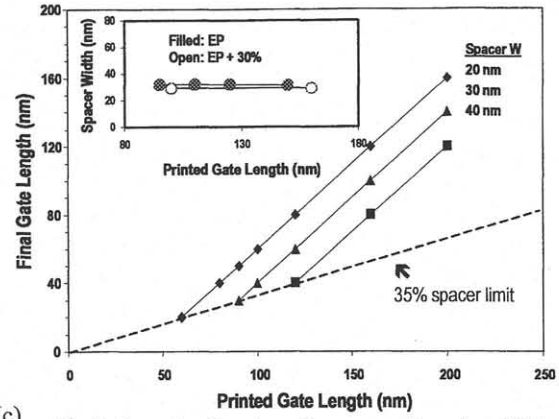


Fig.2: Lg reduction: keeping spacer/trench < 35%, ArF phase-shift lithography can yield 25 nm final Lg. Insert: spacer width (30 nm as deposited) is insensitive to overetching and printed Lg [2].

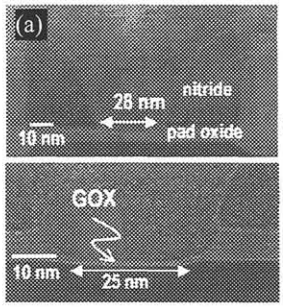


Fig. 3: TEM of mechanical SALVO structure: (a) inner spacers on pad oxide, with opening of 28 nm; (b) V-gate with 1.9nm gate oxide and channel length of 25 nm.

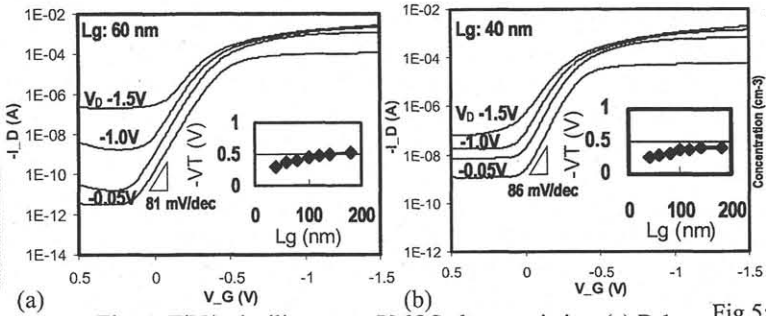


Fig. 4: TiN/polysilicon gate PMOS characteristics: (a) B 1 keV S/D implant: 60 nm Lg with S of 81 mV/decade, ≤2 mV/nm $V_T$ roll-off and $I_{on}/I_{off}$ of $10^5$; (b) B 0.5 keV S/D implant: 40 nm Lg device with S of 86 mV/decade, ≤2 mV/nm $V_T$ roll-off and $I_{on}/I_{off}$ of $10^4$ [2].

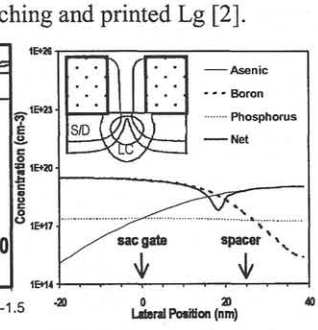


Fig.5: PMOS channel doping simulation shows that As LC implant produces sharp (8.4 nm/decade) lateral profiles, after gate RTA [1].

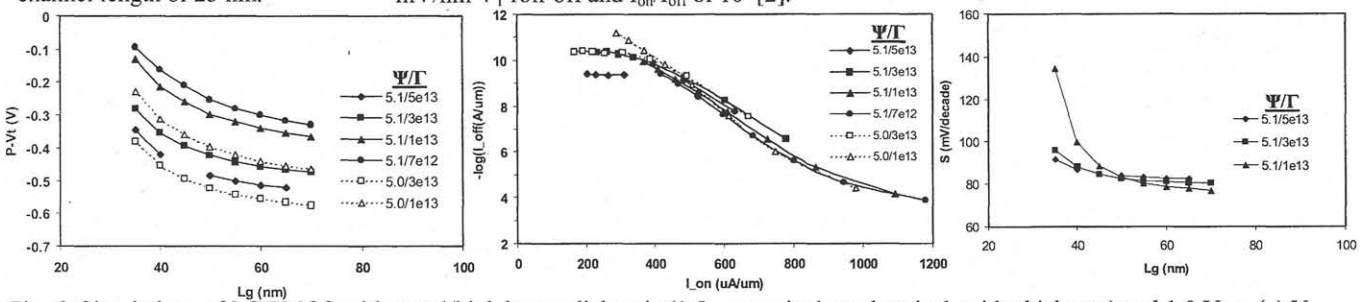


Fig. 6: Simulations of LC PMOS with metal/high k gate dielectric (1.5 nm equivalent electrical oxide thickness) and 1.0 $V_{DD}$: (a) $V_T$ characteristics as functions of Lg, metal workfunction Ψ and LC implant dose Γ; (b) As 3e13 $cm^{-2}$ produces the best $I_{on}$ of 750 μA/μm at $I_{off}$ of 160 nA/μm; (c) sub-threshold slopes are good (≤ 95 mV/decade) for sub-50 nm gates except with high LC dose.

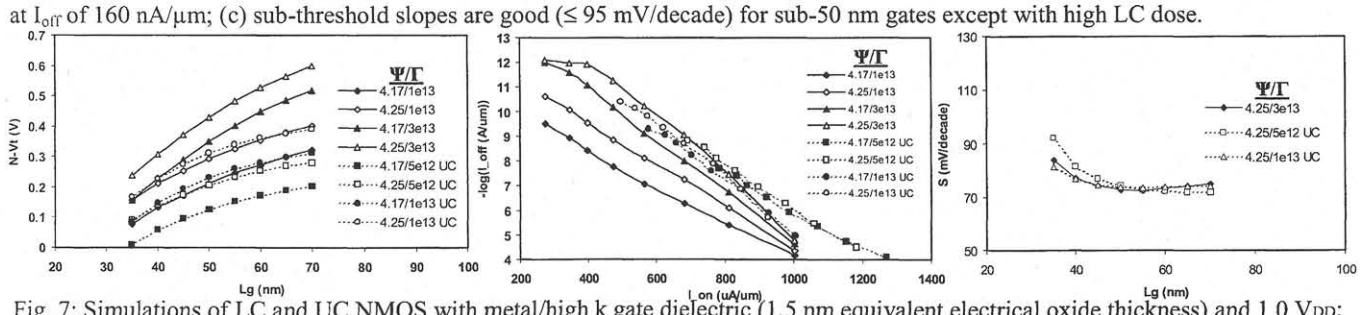


Fig. 7: Simulations of LC and UC NMOS with metal/high k gate dielectric (1.5 nm equivalent electrical oxide thickness) and 1.0 $V_{DD}$: (a) $V_T$ characteristics as functions of Lg, metal workfunction Ψ and implant dose Γ; (b) UC of $BF_2$ 5e12 $cm^{-2}$ produces the best $I_{on}$ of 920 μA/μm at $I_{off}$ of 160 nA/μm; (c) sub-threshold slopes are excellent (≤ 90 mV/decade) for sub-50 nm gates.