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80 nm High Performance CMOSFET with Low Gate Leakage Current Using Conventional Thin Gate Nitric Oxide

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1. Introduction

Recently, the size of MOSFET's has been shrunk to realize high-performance integrated circuit. Gate oxide thickness for high performance MOSFET is downscaled aggressively. The gate-drain leakage current contained in the stand-by current of MOSFET with sub 3nm-thick gate oxide is not negligibly small. Instead of the gate oxide, high-K insulator film has been proposed to apply to the fabrication of silicon device in order to reduce the gate leakage current. However, the technology that can suppress the gate leakage current without high-K insulator is expected, since high-K insulator has less compatibility to the conventional silicon process technology. We propose that gate overlap should be downscaled as well as gate oxide thickness because gate leakage current contained in the stand-by current will be in proportion to the gate overlap area. Gate overlap area is controlled by the offset sidewall width for source drain extension (SDE) implantation [1,2]. In this paper, it is shown that gate leakage current contained in the stand-by current can be controlled by using offset SDE implantation and that low stand-by current FET with conventional gate oxide can be fabricated without high-K gate insulator. In addition, it is also indicated that double offset implantation technique of SDE [3] can optimize the offset spacer widths for both pFET and nFET. As a result, 80nm CMOSFET of high performance and low stand-by current has been realized.

2.Experiment

Figure 1 shows the double offset-implanted SDE process. The 1st offset sidewall spacer was fabricated by etch-back method of CVD oxide. N-SDE was formed by arsenic ion implantation. After 10nm oxide film was deposited as the second offset spacer, BF_2 ions were continuously implanted into the film. The implantation dose is so high that p-SDE was formed by solid phase diffusion from the BF_2-doped oxide film at the activation RTA. At the end of process, the gate-source/drain overlap lengths for nFET and pFET were about 20 and 10nm, respectively.

3. Results and discussion

Offset-spacer width dependence of gate-drain leakage current is shown in Fig.2. The leakage current decreases with an increase in the offset spacer width. The leakage current of MOSFET's with 14nm-offset spacer is reduced to 1/5 as low as that of MOSFET's with no offset spacer. For most CMOS integrated circuits, the channel width of pFET's is usually about twice as large as nFET's. Therefore, PMOSFET should be evaluated to have twice as high leakage current as the measured data shown in Fig. 2(b). In the case that the 1st offset spacer width is set to 10nm and the 2nd one is set to 10nm, the gate leakage current can be suppressed less than 20pA/um. Ion-Ioff characteristics of 120nm FET's are shown in Fig. 3. It should be noted that off-state leakage current reduces with an increase in the width of the offset spacer. An off-state leakage current of 20pA/um can be achieved by 14nm offset spacer, since the 14nm offset spacer suppresses the gate-drain leakage current.

Figure 4 shows the offset spacer width dependence of DIBL at 80nm MOSFET. With an increase in the offset spacer width, DIBL is improved drastically.

Figure 5 depicts the cross-sectional SEM image of 80nm MOSFET. Figures 6-7 exhibit Ion-Ioff, threshold voltage roll-off characteristics of 80nm CMOSFET fabricated by the double offset spacer technology, respectively.

The gate-source/drain overlap capacitance is decreased with an increase in the offset spacer width as shown in Fig. 8. In Fig. 8(b), the capacitance of pFET is twice larger than the measured data for the same reason as the gate leakage current. Since the gate overlap capacitance can be the dominant factor for the integrated circuit speed, the decrease in the overlap capacitance is important to realize high performance devices. However, the drain current of nFET is decreased with an increase in the offset spacer width as shown in Fig.9 (a). On the other hand, the drain current of pFET is not dependent upon the offset spacer width as shown in Fig.9 (b). Figure 10 shows the dependence of (Cov + α)/Ids on off current. α represents the circuit capacitance except for gate overlap capacitance. (Cov + α)/Ids is an index of gate delay time. In the case of α=0fF/um, delay time of both nFET and pFET decrease with an increase in offset sidewall width in all the Ioff conditions reflecting the decrease in gate overlap capacitance. In the case of α=5fF/um, the delay time of pFET decreases with an increase in offset spacer width in all the Ioff conditions. On the contrary, the delay time of nFET increases with an increase in the offset spacer width in over-10pA ioff condition reflecting the decrease in the drain current. Therefore, the optimum spacer width is different from nFET and pFET. To evaluate the above-mentioned tendency, the intrinsic gate delay time of ring oscillator consisted of inverter chain (F.O.=1, Ioff=10nA/um) is simulated as shown in Fig.11. The gate delay time (Tpd) is improved according to the decrease in the 1st offset spacer width. However, the improvement ratio of Tpd versus offset spacer width satulates in the over-12nm region. This is because the reduction of overlap capacitance is cancelled by the degradation of the nFET drain current. In the case of double offset spacer structure, Tpd is further improved. This is because the drain current of nFET is maintained high and the overlap capacitance of pFET decreases drastically. Since the overlap capacitance of pFET is a dominant factor in the Tpd, it is very important to reduce the overlap capacitance to realize high-speed circuits. Double offset spacer technology enables to fabricate nFET with high drain current and pFET with low overlap capacitance, and thus, high performance CMOSFET.

4. Summary

High performance CMOSFET with 80nm gate length has been fabricated by using double offset SDE implantation technique. Double offset sidewall spacer structure reduces the gate-drain leakage current drastically. At the same time, circuit performance is improved by decreasing gate-drain overlap capacitance while maintaining the high drive current. Double offset implantation is a key technology to realize high performance 80nm integrated circuits.

References

1. K. F. Lee et al, IEDM, pp.1012 (1992)
2. S. Thompson et al, VLSI symp., pp.132 (1998).
3. H. Sayama et al, IEDM, pp.239 (2000)

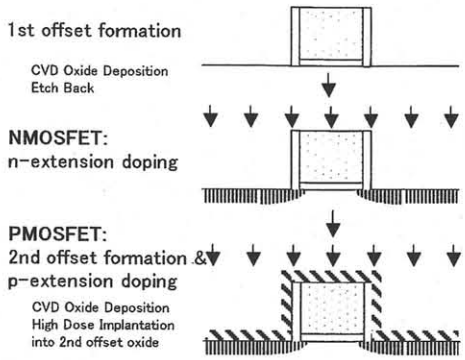

Fig. 1 Double offset spacer implantation process

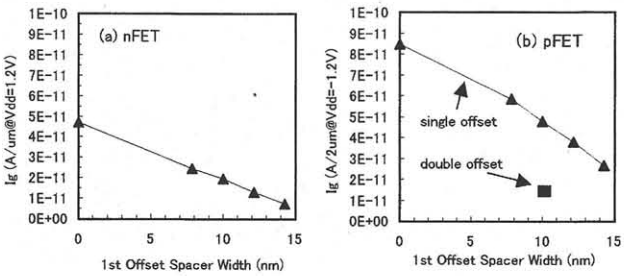

Fig. 2 Dependence of gate leakage current on 1st offset width

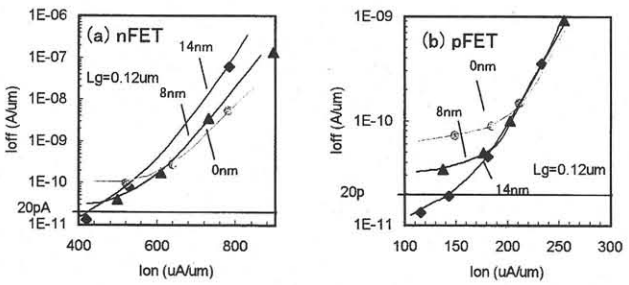

Fig.3 IonIoff charactristics of nFET and pFET with various 1st offset spacer width

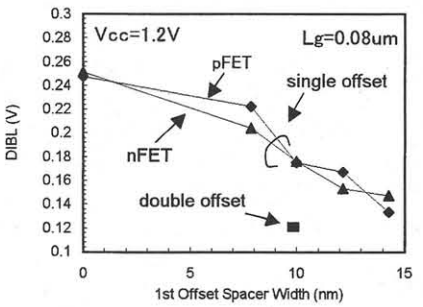

Fig. 4 Dependence of DIBL on 1st offset spacer width

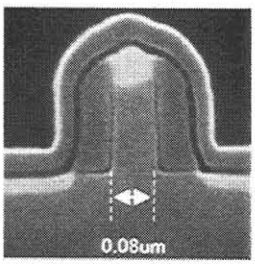

Fig. 5 Cross sectional SEM image of 80nm MOSFET with double offset

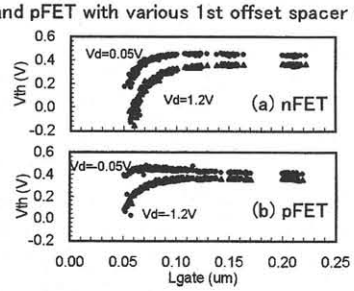

Fig. 6 Gate length dependence of threshold voltage, of nFET and pFET with double offset

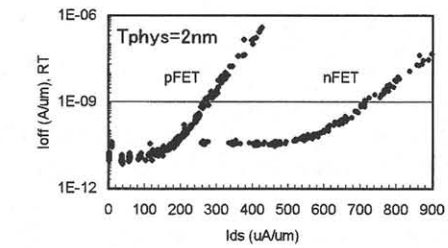

Fig. 7 IonIoff charactristics (Vcc=1.2V) of nFET and pFET with double offset spacer structure

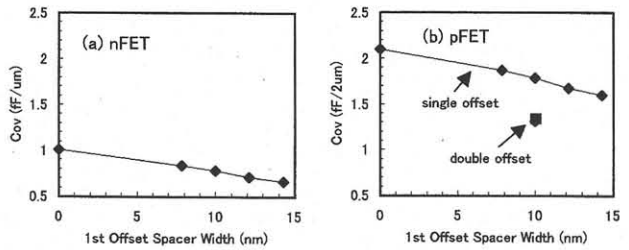

Fig. 8 Dependence of gate overlap capacitance on 1st offset sidewall spacer width

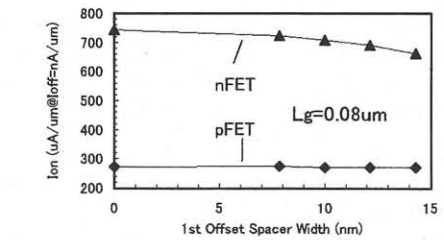

Fig. 9 Dependence of drive current (at Ioff=1nA/um) on 1st offset spacer width

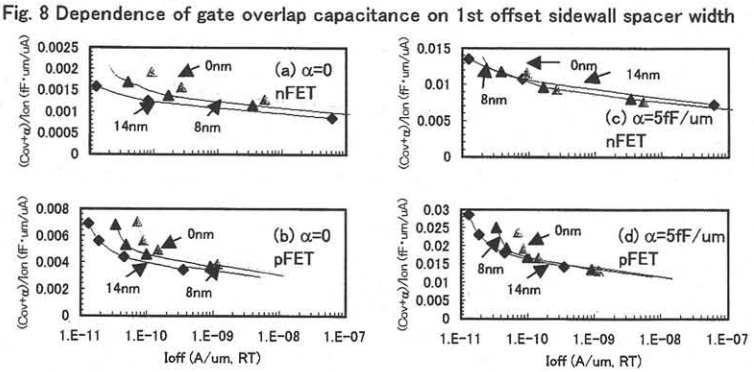

Fig. 10 (Cov+A)/Ion versus Ioff is plotted for offset spacer width of 0, 8, 14nm. α means the parastic capacitance except for gate overlap one. (Cov+α)/Ion represents the gate delay time.

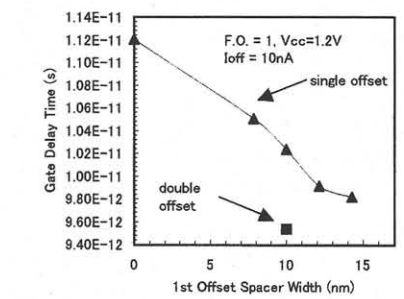

Fig. 11 Gate delay time dependence on the 1st offset spacer width