F-2-2
80 nm High Performance CMOSFET with Low Gate Leakage Current Using Conventional Thin Gate Nitric Oxide

K. Ota, H. Sayama, H. Oda, Y. Inoue and M. Inuiishi

ULSI Development Center, Mitsubishi Electric Corporation, 4-1 Mizuhara, Itami, Hyogo 664-8641, Japan

ULSI Process Technology Development Center, Semiconductor Company, Matsushita Electric Industrial Corporation, 19 nishikujyo-kasagachlo, Minami-ku, Kyoto, 601-8413, Japan

1. Introduction

Recently, the size of MOSFET's has been shrunken to realize high-performance integrated circuit. Gate oxide thickness for high performance MOSFET is downscaled aggressively. The gate-drain leakage current contained in the stand-by current of MOSFET with sub 3nm-thick gate oxide is not negligibly small. Instead of the gate oxide, high-K insulator film has been proposed to apply to the fabrication of silicon device in order to reduce the gate leakage current. However, the technology that can suppress the gate leakage current without high-K Insulator has less compatibility to the conventional silicon process technology. We propose that gate overlap should be downscaled as well as gate oxide thickness because gate leakage current contained in the stand-by current will be in proportion to the gate overlap area. Gate overlap area is controlled by the offset sidewall width for source drain extension (SDE) implantation [1,2]. In this paper, it is shown that gate leakage current contained in the stand-by current can be controlled by using offset SDE implantation and that low stand-by current FET with conventional gate oxide can be fabricated without high-K gate insulator.

In addition, it is also indicated that double offset implantation technique of SDE [3] can optimize the offset spacer widths for both pFET and nFET. As a result, 80nm CMOSFET of high performance and low stand-by current has been realized.

2. Experiment

Figure 1 shows the double offset-implanted SDE process. The 1st offset sidewall spacer was fabricated by etch-back method of CVD oxide. N-SDE was formed by arsenic ion implantation. After 10nm oxide film was deposited as the second offset spacer, BF$_2$ ions were continuously implanted into the film. The implantation dose is so high that p-SDE was formed by solid phase diffusion from the BF$_2$-doped oxide film at the activation RTA. At the end of process, the gate-source/drain overlap lengths for nFET and pFET were about 20 and 10nm, respectively.

3. Results and discussion

Offset spacer width dependence of gate-drain leakage current is shown in Fig.2. The leakage current decreases with an increase in the offset spacer width. The leakage current of MOSFET's with 14nm-offset spacer is reduced to 1/5 as low as that of MOSFET's with no offset spacer. For most CMOS integrated circuits, the channel width of pFET's is usually twice as large as nFET's. Therefore, PMOSFET should be evaluated to have twice as high leakage current as the measured data shown in Fig. 2(b). In the case that the 1st offset spacer width is set to 10nm and the 2nd one is set to 10nm, the gate leakage current can be suppressed less than 20pA/um. Ion-Ioff characteristics of 120nm FET's are shown in Fig. 3. It should be noted that off-state leakage current reduces with an increase in the width of the offset spacer. An off-state leakage current of 20pA/um can be achieved by 14nm offset spacer, since the 14nm offset spacer suppresses the gate-drain leakage current.

Figure 4 shows the offset spacer width dependence of DIBL at 80nm MOSFET. With an increase in the offset spacer width, DIBL is improved drastically.

4. Summary

High performance CMOSFET with 80nm gate length has been fabricated by using double offset SDE implantation technique. Double offset sidewall spacer structure reduces the gate-drain leakage current drastically. At the same time, circuit performance is improved by decreasing gate-drain overlap capacitance while maintaining the high drive current. Double offset implantation is a key technology to realize high performance 80nm integrated circuits.

References
1. K. F. Lee et al, IEDM, pp.1012 (1992)
1st offset formation
CVD Oxide Deposition
Etch Back
NMOSFET: n-extension doping
PMOSFET: 2nd offset formation & p-extension doping
CVD Oxide Deposition
High Dose Implantation into 2nd offset oxide

Fig. 1 Double offset spacer implantation process
Fig. 2 Dependence of gate leakage current on 1st offset width
Fig. 3 Ionloff characteristics of nFET and pFET with various 1st offset spacer width
Fig. 4 Dependence of DBL on 1st offset spacer width
Fig. 5 Cross sectional SEM image of 80nm MOSFET with double offset
Fig. 6 Gate length dependence of threshold voltage of nFET and pFET with double offset
Fig. 7 Ionloff characteristics (Vcc=1.2V) of nFET and pFET with double offset spacer structure
Fig. 8 Dependence of gate overlap capacitance on 1st offset sidewall spacer width
Fig. 9 Dependence of drive current (at Ioff=1mA/um) on 1st offset spacer width
Fig. 10 (Cov+α)/Ion versus Ion is plotted for offset spacer width of 0, 8, 14nm. α
means the parasitic capacitance except for gate overlap one. (Cov+α)/Ion
represents the gate delay time.

Fig. 11 Gate delay time dependence on the 1st offset spacer width