Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, Tokyo, 2001, pp. 150–151

F-2-3

Elevated Extension Structure for 35 nm MOSFETs

Yoshiki Kamata, Mizuki Ono and Akira Nishiyama
Advanced LSI Technology Laboratory, Corporate R&D Center, Toshiba Corporation
Phone: +81-45-770-3691, Fax: +81-45-770-3578 e-mail: yoshiki.kamata@toshiba.co.jp
8 Shinsugita-cho, Isogo-ku, Yokohama, 235-8522 JAPAN

Abstract

A novel extension structure using in-situ doped selective silicon formation is proposed. Using device simulation we show the design guideline of this structure for the minimization of the propagation delay of 35nm CMOS devices. Eventually, this structure proves itself to have a better cut-off characteristic and higher current drive than the already reported comparable MOSFET.

1. Introduction

Shallow extension structure is required for the realization of sub-100nm CMOS transistors. There are many candidates for its formation [1-4], however none of them have satisfied the ITRS requirements [5] for the junction depth (X_j) and the sheet resistance for 70nm node CMOS and further generations so far. Therefore, we propose the application of highly doped selective silicon formation and solid state diffusion for the realization of very shallow extensions with low sheet resistance as in Fig. 1. In-situ doped selective Si and SiGe formations have already been reported [6-7]. The newly proposed structure uses the in-situ doped silicon layer as the elevated extension and contact source/drain region by one step selective formation as in the process sequence (Fig. 2). In order to accomplish extremely shallow junctions with low sheet resistance, the extensions are elevated. Hence this structure *might* suffer from a large parasitic capacitance between gate and source/drain (C_{para}). We investigated the influence of the structural parameters on the parasitic capacitance and the extension resistance and successfully obtained a set of optimum parameters in terms of the CMOS gate delay.

2. Structure in Simulation

A three-dimensional device simulator (DIAMOND) was used in this study. An elevated extension structure and typical device parameters are depicted in Fig. 1. The gate electrode is made of n+-poly silicon and the substrate doping concentration (N_{sub}) is uniformly $3x10^{18}$ cm^{-3}. The extension region consists of two parts. The upper part is the in-situ doped silicon region with the impurity concentration of $4x10^{20}$ cm^{-3}. The lower part is the diffusion layer in the silicon substrate. Figure 3 (a) shows phosphorous concentration SIMS profiles for samples, in which the impurity atoms were doped by solid phase diffusion from the doped silicon layer with the impurity concentration of $4x10^{20}$ cm^{-3} deposited by CVD at 600°C. RTA at 800°C for 10 seconds resulted in the junction depth of 11nm at $3x10^{18}$ cm^{-3} (Fig. 3 (b)). Furthermore the leakage current level of this shallow junction was well suppressed as in Fig.4. Therefore we used the phosphorous profile of this condition as the diffusion layer in the silicon substrate. The measured resistivity of doped silicon layer as low as 1mΩcm was also implemented in this simulation. We calculated the propagation delay time changing the distance between the gate and the elevated extension (Y_{gd}) and the extension thickness (X_{EE}). We also optimized the silicon thickness (X_{elev}) outside the silicon nitride sidewall and the sidewall thickness (Sw2).

3. Results and Discussion

Figure 5 shows a comparison of I_{ds}-V_g characteristics between this elevated extension device with typical structural parameters (see caption and Fig. 1) and the already reported 30nm device in ref. 8. This figure shows a better cut-off characteristic and a higher current drive in the newly proposed structure. Optimizations of the structural parameters are mentioned in detail as follows. Figures 6 and 7 show that I_{ds} and C_{para} increase when X_{EE} increases. I_{ds} increases up to X_{EE} value of 6nm and saturates for farther X_{EE} increase. It has been revealed that the increase of the capacitance component C_2 between elevated extension and gate (inset Fig. 7) can be well explained by the parallel plate approximation. The optimized X_{EE} is around 5nm in terms of the reduction of t_{pd} (CMOS inverter) as in Fig. 8. This optimized X_{EE} didn't change for various X_{elev} and Sw2 values. Figure 9 shows Y_{gd} dependence of t_{pd} with X_{EE} as a parameter. It can be seen that t_{pd} increases drastically with Y_{gd} over 6nm. This phenomenon can be explained by the steep decrease of I_{ds}, and indicates that the gate/diffusion-region overlap Y_j of at least 5nm is required for large I_{ds} (inset Fig.9). Figure 10 shows that the dependences of S-factor and V_{th} on Y_{gd} are weak, indicating that the extremely precise Y_{gd} control is not required. Figure 11 shows that there are local minima of t_{pd} with respect to Sw2. This phenomenon can be explained by the increase of parasitic resistance and the decrease of C_{para} with Sw2 increase. The Sw2 value which realizes the minimum t_{pd} slightly increases with X_{elev}. t_{pd} increases monotonically with the X_{elev} increase. We selected 100nm for the minimum X_{elev} in order to retain a distance between the silicide and pn-junction for the suppression of pn-junction leakage current increases [9-10]. Optimum regions of structural parameters considering 5% increase of t_{pd} are summarized in Table 1(a). Table 1 (b) shows electrical properties of the optimized 35nm device. The gate delay comparable to that of 50nm technology node (L_g=32 nm, high performance) was successfully obtained.

4. Conclusions

It has been shown that the novel extension structure using in-situ doped selective silicon formation can realize

excellent performances of MOSFETs of 35nm and farther generations.

References

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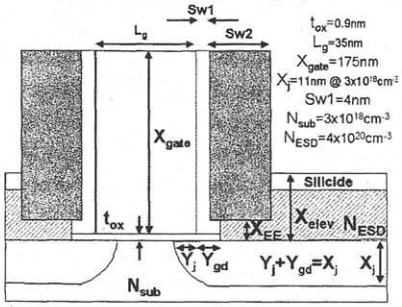

Fig.1 Structure and typical device parameters of MOSFET with elevated extension (shadow area represents in-situ doped silicon layer)

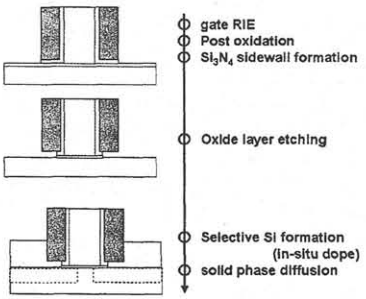

Fig.2 Process sequence of MOSFET fabrication with in-situ doped selective silicon formation

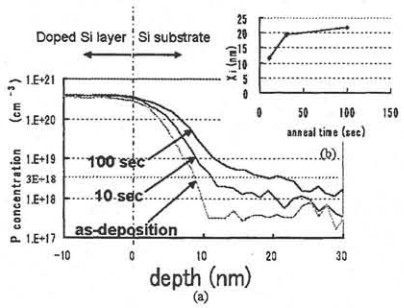

Fig.3 (a) Phosphorous concentration SIMS profile for as-deposited and after diffusion by 800℃ RTA
(b) Junction depth at 3x10^{18} cm^{-3} as a function of annealing time
(Depth is measured from the original surface before silicon deposition.)

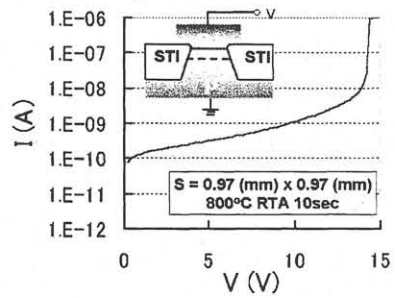

Fig.4 Current-voltage characteristic of n+/p junction formed by solid phase diffusion from doped silicon region (800°C RTA 10sec)

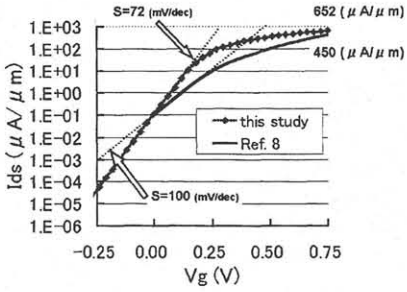

Fig.5 I_{ds}-V_g characteristics of 35nm MOSFET with the optimized device parameters (V_d=0.75V, X_{EE}=5nm, Y_{gd}=5nm, Sw2=50nm, X_{elev}=100nm) and 30nm device of ref.8 (T_{ox}=0.8nm, V_d=0.85V)

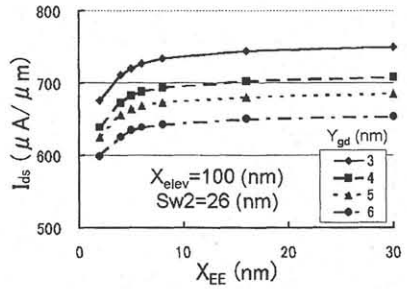

Fig.6 X_{EE} dependences of I_{ds} with Y_{gd} as a parameter

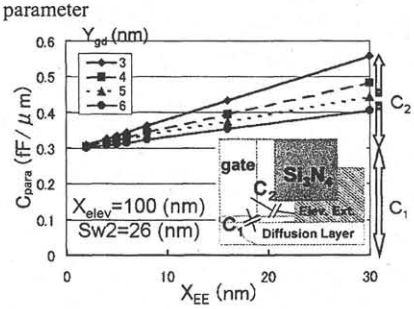

Fig.7 X_{EE} dependences of C_{para} with Y_{gd} as a parameter

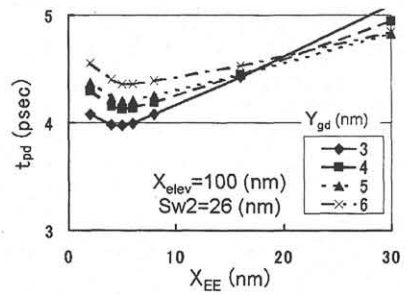

Fig.8 X_{EE} dependence of t_{pd} (CMOS inverter) with Y_{gd} as a parameter

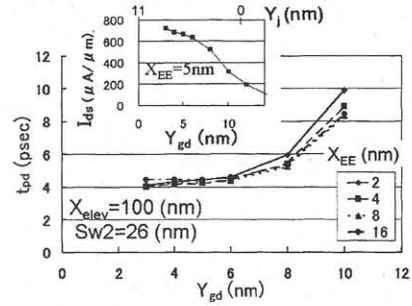

Fig.9 Y_{gd} dependence of t_{pd} with X_{EE} as a parameter
(Inset: Y_{gd}, Y_j dependence of I_{ds} in the case of X_{sw}=5nm)

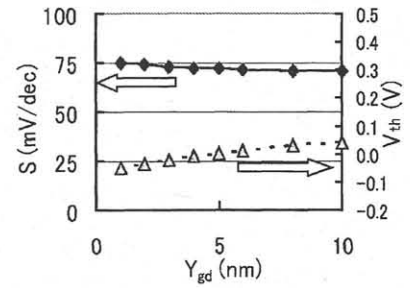

Fig.10 Y_{gd} dependence of S-factor and V_{th} (X_{EE}=5nm, Sw2=26nm and X_{elev}=100nm. Other parameters are depicted in Fig.1)

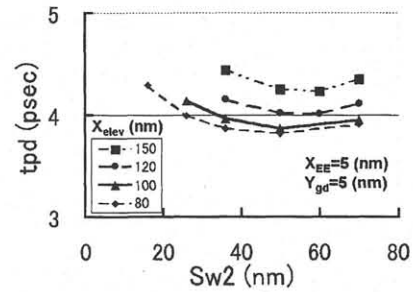

Fig.11 Sw2 dependence of t_{pd} with X_{elev} as a parameter

Table.1 (a) Optimal ranges of structural parameters extracted from the t_{pd} degradation of 5%
(b) Electrical properties of 35nm MOSFET with optimized structural parameters (X_{EE}=5nm, Y_{gd}=5nm, Sw2=50nm and X_{elev}=100nm.Other parameters are depicted in Fig.1)

(a)

X_{EE}	5±4 (nm)
Y_{gd}	< 6 (nm)
Sw2	50±20 (nm)
X_{elev}	100~130 (nm)

(b)

I_{ds}	652 (μA/μm)
t_{pd}	3.9 (psec)
S-factor	72 (mV/dec)
$\Delta V_{th}/\Delta L_g$	2.3 (mV/nm)