Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, Tokyo, 2001, pp. 152–153

F-2-4

A T-Gate MOSFET with Reduced Channel Length by Inverted Sidewalls for Sub-100 nm RF Applications

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Introduction

RF CMOS has attracted a lot of interests in recent years as its high frequency figures of merit keep improving via scaling. As the gate length is reduced to the sub-100nm regime, however, the gate resistance will inevitably increase since thick silicide is difficult to realized. Large gate resistance can severely degrade the f_{max} and offset the gain in NF_{min}. While the fingered structure has been commonly used to reduce the gate resistance, this scheme could not solve all the problems due to the increase in parasitic capacitance. For this reason, T-gate structures or metal gates for MOSFETs have been proposed by different research groups [1][2][3]. The T gate approaches involve the selective overgrowth of either W or silicon to form the desired gate shapes and thus significantly increase the complexity of processing. More importantly, the controllability of the upper gate length is not guaranteed. While metal gates can avoid this problem, their scalability into the sub-100nm regime is a concern [4].

In this paper, we propose a manufacturable and fully self-aligned T-gate structure for sub-100nm generation, as shown in Fig 1. In this structure, the upper gate length is completely decoupled from the reduced channel length $L_{reduced}$ and this allows a much larger design window for reducing the gate resistance. Meanwhile, the very short channel length, which is required to boost cut-off frequency, is achieved without using extreme lithography system. Here, the effective drawn gate channel length is significantly reduced by the doped inverted sidewalls and the self-aligned source/drain extensions formed by solid phase diffusion. To fabricate this structure, only one extra mask is required and this makes it a robust approach for high performance RF CMOS. In this work, the main ideas of this structure are demonstrated.

Device Fabrication

Fig 2 and Fig 3 show the key process steps and the illustrations of the doped inverted sidewall formation. After LOCOS isolation, a LTO layer of 250nm was deposited. Following the equivalent gate level lithography, reactive ion etching was used to form the replacement LTO column as shown in Fig 3-1. This LTO column defined the length of the trench which would be used for the formation of the inverted sidewalls. At this point, the wafers were ready to accept source/drain implantation with $5x10^{15}cm^{-2}$ As at 25KeV. Then a layer of ~500nm silicon nitride was deposited followed by planarization. The silicon nitride thickness was further thinned down by wet etch in 150°C phosphoric acid until a desired thickness had been reached. This desired thickness determines partly the final width of the inverted sidewall. The trench formation was completed with the removal of the LTO column in BOE. Afterward, the PSG inverted sidewalls were formed by depositing 140nm of PSG followed by RIE etchback as shown in Fig 3-3. While PSG was used in this study, the inverted sidewalls could be made of other dielectric materials on top of a thin layer of implanted oxide as a diffusion source to further improve the controllability [5]. In the case of PMOS, implanted oxide with boron can used to replace BSG. Following the threshold voltage adjustment implant, 3.0 nm gate oxide was grown at 800°C in diluted oxygen for 15 minutes. The gate was finished by depositing polysilicon and RIE. Finally, the samples were annealed at 950°C for 15 seconds, mainly for driving the phosphorous to formed the source/drain extensions. A cross sectional SEM picture of the device structure is shown in Fig 4. It can be noticed that the sidewall of the trench is inclined slightly inward because the RIE etching of the LTO was not perfectly anisotropic.

Device characteristics

As mentioned before, the bottom gate length is shrunken by the inverted sidewalls. Therefore, the reduced defined channel length is equal to $L_{reduced} = L_{trench} - 2L_{spacer}$, where L_{trench} and L_{spacer} are the length of the trench and the doped LTO sidewalls respectively. Fig 4 shows a sample with the trench length of 200nm and the subsequent channel length is reduced to about 70nm. Fig 5 shows the V_{th} and DIBL versus the initial trench length respectively. As shown, the V_{th} is well controlled even down to a $L_{reduced}$ of 40nm. Furthermore, no V_{th} roll-up is observed since the source/drain implantation was formed well before the V_{th} adjustment implant and the source /drain extensions were implemented by solid phase diffusion. Similarly, DIBL has been kept small down to a $L_{reduced}$ of 40nm where it is approximately 80mV/V. Fig 6 shows the SIMS profile of the junction formed by solid phase diffusion from the PSG. The profile for 800°C annealing shows that the diffusion of phosphorous is still quite limited during the oxidation. Therefore, a high temperature anneal is required to drive in the phosphorous, and the junction depth and sheet resistance of the extensions can be optimized by adjusting the annealing time. Fig 7 and Fig 8 show the typical subthreshold and output characteristics of this structure. The demonstrated sample has a reduced channel length of 70nm. The device has excellent subthreshold behaviors of small DIBL and S-factor (50mV/V and 88mV/decade respectively). Also, no conspicuous leakage current is observed even though the PSG is used as the sidewall material. The Id_{sat} is 3.2mA at Vd=Vg=2V. The slightly lower Id_{sat} than reported in the literatures with comparable gate length and gate oxide occurs because silicide is not used for the source/drain junctions in the current experiments. Fig 9 shows the $G_{m,max}$ versus the initial trench length. As shown, the transconductance keeps increasing down to L_{gate} of ~40nm. This shows that formation of the inverted sidewalls is trench width scalable. To further improve the device performance, thermally stable W silicide on source/drain junctions can be used to lower the sheet and contact resistances. As shown in Fig 10, even with slightly higher resistive W salicide, the reduced source/drain resistance has significantly improved the current drive. Fig 11 shows the simulated f_{max} versus the top gate length, with different values of sheet resistance for the silicided gate. The finger length is set to a relatively long 5μm so that C_{gb} can be neglected. As can be seen, f_{max} is significantly improved with a wider top gate length.

Conclusions

In this paper, we have demonstrated the key idea of a fully self-aligned T-gated MOSFET with inverted sidewalls down to the sub-100nm regime. The manufacturable T gate and the easily attainable small gate length have made it a promising candidate for CMOS RF applications.

References

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[3] A. Chatterjee et al, IEDM, pp.821(1997)
[4] E.Josse et al., IEDM, pp. 661 (1999)
[5] J. Schmitz et al., IEDM, pp. 1009 (1998)

Acknowledgment

This project is funded by DARPA.

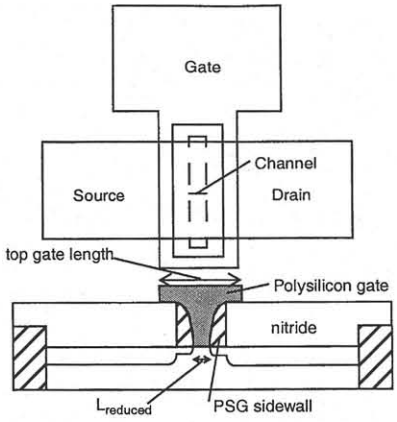


Fig 1. Schematic diagrams of the T-gated MOSFET with inverted sidewalls. Top and cross sectional views.

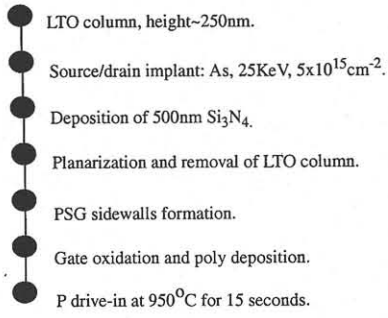


Fig 2. Key process steps.

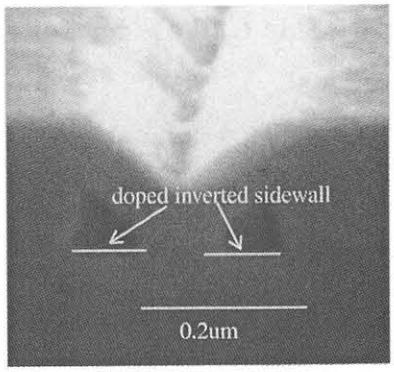
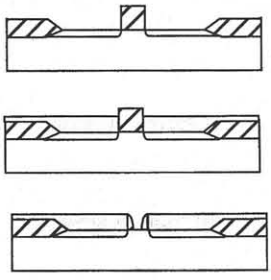


Fig 4. Cross sectional SEM picture of a T-gated MOSFET with a physical gate length of 70nm.



1. A LTO column is defined by lithography and RIE etching.

2. A thick layer of nitiride is deposited and then planarized. The final thickness is controlled by wet etch using phosphoric acid.

3. A trench is formed when the LTO column is removed by BOE and PSG sidewalls are formed by deposition and etchback.

Fig 3. Illustration of the formation of the inverted sidewalls.

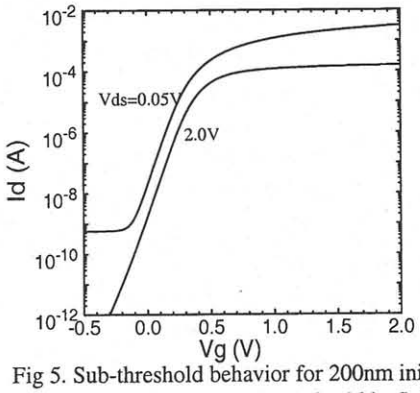


Fig 5. Sub-threshold behavior for 200nm initial trench length and 10μm channel width. S-factor~88mV/decade. Lg~70nm.

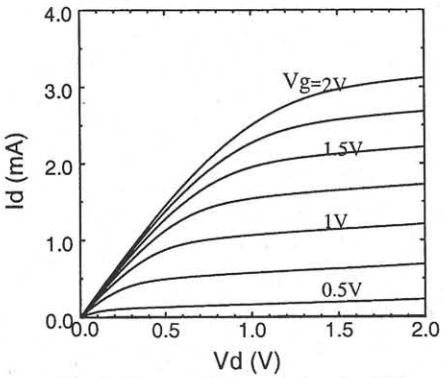


Fig 6. Output characteristics for 200nm initial trench length and 10μm channel width. Lg~70nm.

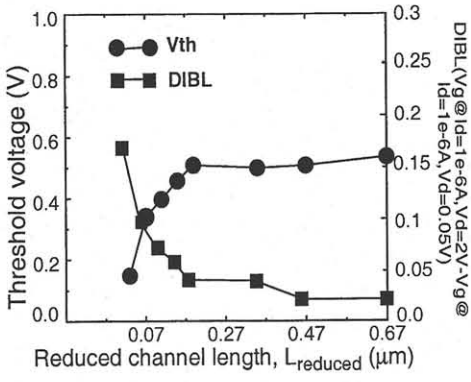


Fig 7. Threshold voltage and DIBL vs. reduced channel length.

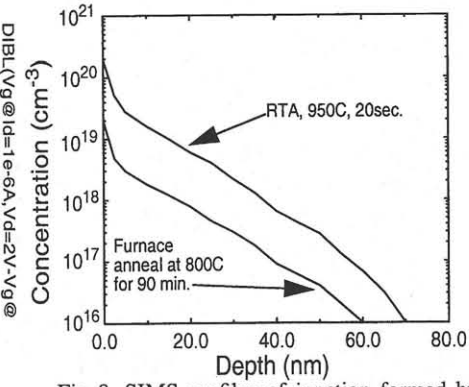


Fig 8. SIMS profiles of junction formed by solid-phase diffusion from PSG.

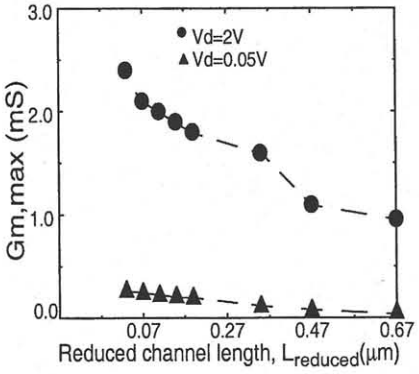


Fig 9. Gm,max(@Vd=0.05V, 2V) vs. reduced channel length.

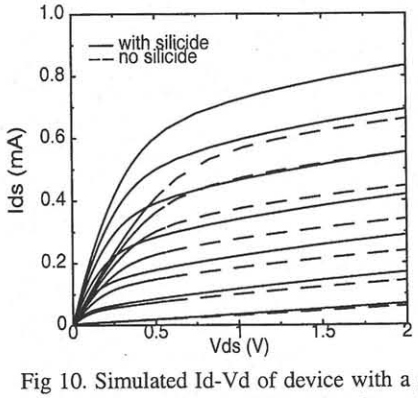


Fig 10. Simulated Id-Vd of device with a gate length of ~40nm. Vgs-Vth varies from 0 to 1.5V (0.25V step).

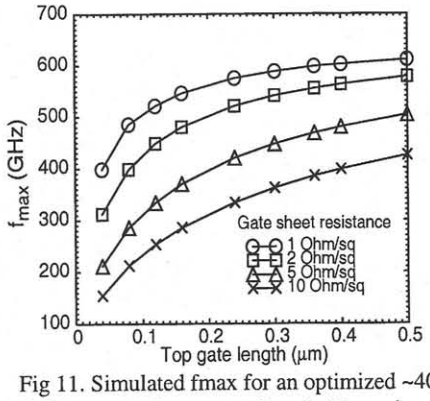


Fig 11. Simulated fmax for an optimized ~40nm device versus the top gate length. Finger length is assumed to be 5μm.