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Side-Gate Design for 50 nm Electrically Induced Source/Drain MOSFETs

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1. Introduction

For the realization of sub-100nm MOSFETs without short channel effects, there have been many works concerning the operation and the characterization of the side-gate MOSFET that has the inversion layer drain structure [1, 2]. The reported MOSFET devices that use an electrically induced inversion layer as a source/drain extension region show an effective suppression of the short channel effects in comparison with conventional MOSFETs. We focus on the device design of a biased side-gate MOSFET with a 50nm main-gate. As shown in Fig. 1, the two side-gates that are formed by doped poly-silicon sidewall spacers induce the inversion layers. The designed side-gate MOSFET device is investigated in terms of the performance including short channel effects due to the biased side-gate. This approach promises an optimized condition in this device structure.

2. Device Design

Fig. 2 illustrates the key process steps for side-gate MOSFET. This process sequence is compatible with conventional MOSFET fabrication flow. In particular, there are two major different processes for side-gate MOSFET; 1) n^+ poly-Si etch-back process for side-gates that induce inversion layers as source/drain extension region, 2) side-gate oxide and inter-gate oxide growth using the oxidation rate difference between bulk Si surface and doped poly-Si. As_2^+ low energy implantation process was adopted to realize source/drain region of 20nm junction depth [3].

Two-dimension and two-carrier device simulation was carried out using TMA MEDICI to find the optimized condition for the side-gate length. In our device simulation, the device performance in terms of short channel effects was focused. The selected mobility model was the full energy balance model. In this model, the electron temperature is fed-back into the continuity equations through the temperature dependent model and temperature diffusion model.

Fig. 3 shows the threshold voltage roll-off characteristics depending on the side-gate bias. Despite the variation of side-gate bias condition, it is found that the additional threshold voltage roll-off and drain induced barrier lowering (DIBL) due to side-gate bias stay at a reasonable range for side-gate lengths larger than 50nm. This additional short channel effect should remain as small as possible, because the designed side-gate MOSFETs already have the short channel effect due to a main-gate reduction. Fig. 4 shows I_{ON}-I_{OFF} plot with the variation of side-gate length. I_{ON} is drain saturation current that measured at V_{DS}=1.0V and V_{GS}=1.0V. For side-gate lengths larger than 50nm, the scaling-down of side-gate length in order to increase I_{ON} is shown to be useful without the increment of I_{OFF}. Thus, the side-gate MOSFET with 50nm side-gate length is desirable with respect to I_{OFF} current.

The peak substrate currents are plotted in Fig. 5 as a function of the drain saturation current The side-gate MOSFET in the $L_{side\text{-}gate}$ of 50nm also shows the improvement of the drain currents without the severe increment of substrate current as the side-gate bias varies.

Table I summarizes the characteristics of the designed side-gate MOSFET in comparison with conventional MOSFET. This suggests that we can achieve reduced short channel effect, high I_{ON}/I_{OFF} ratio and low substrate current characteristics by using 50nm channel side-gate MOSFET with 50nm-long side-gates.

3. Conclusions

50nm channel MOSFETs with two side-gates are designed. We propose a side-gate MOSFET compatible with conventional process. Two-dimension and two-carrier device simulation of this side-gate MOSFET shows that the design of the same side-gate length as that of the main-gate promises optimized device characteristics including the immunity to short channel effects. In addition, the designed side-gate MOSFET exhibits a good performance in comparison with conventional MOSFET.

Acknowledgements

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References

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[2] H. Kawaura, et al., *IEEE Trans. on Electron Devices*, Vol. 47, No. 4, p. 856 (2000).

[3] B. Y. Choi, et al., *Ext. Abs. of the Int'l Conf. on SSDM,*

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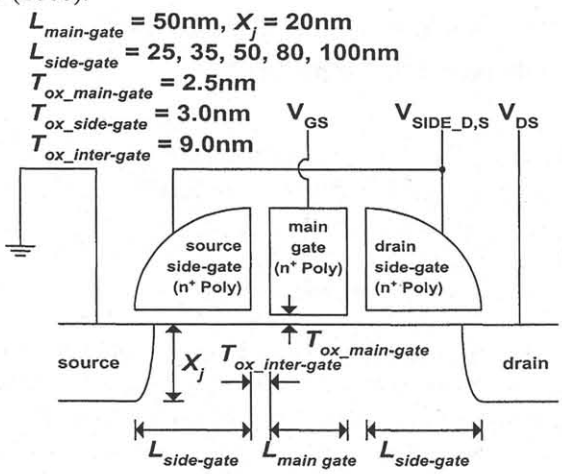

Fig. 1 Biased side-gate MOSFET structure. This side-gate consists of a "drain side-gate" and "source side-gate" is biased independently of main-gate.

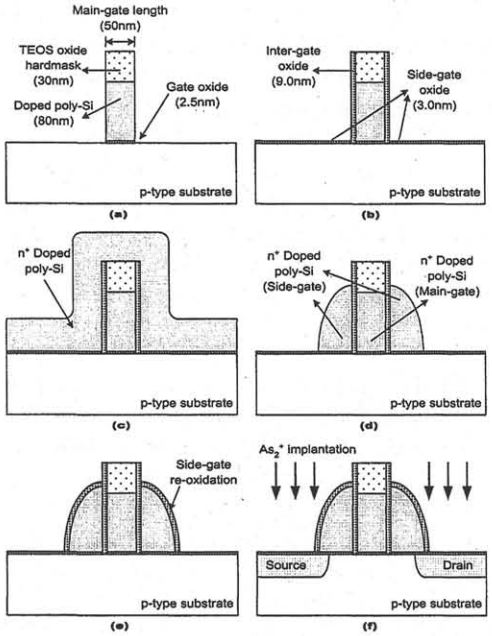

Fig. 2 Key process steps of a designed side-gate MOSFET; (a) gate definition, (b) inter-gate and side-gate oxidation, (c) poly-Si deposition and doping, (d) side-gate formation, (e) side-gate re-oxidation, and (f) source/drain implantation.

Table I Measured characteristics of designed side-gate MOSFET in comparison with conventional MOSFET.

	Side-gate MOSFET	Conventional MOSFET
$L_{main\text{-}gate}$ (nm)	50nm	50nm
Sidewall Spacer	50nm biased poly-Si	Oxide sidewall
DIBL (mV)	3.2	52.3
SS (mV/dec)	82.02	84.56
I_{ON}/I_{OFF}	2.54×10^{6}	0.15×10^{6}
Max. I_{SUB} (A/μm)	1.35×10^{-8}	3.13×10^{-8}

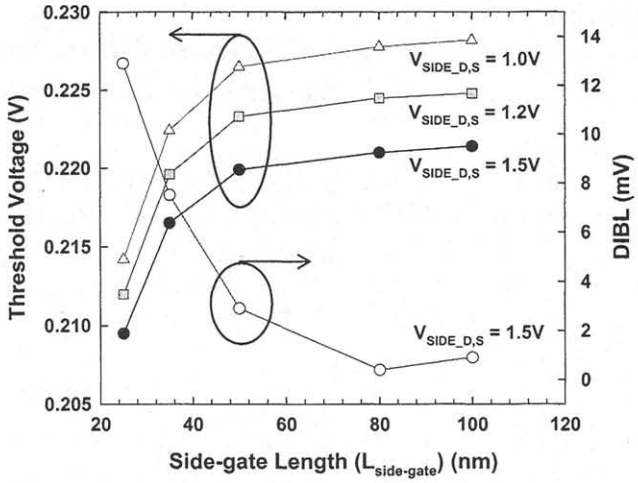

Fig. 3 Threshold voltage roll-off and DIBL as a side-gate length varies from 25nm to 100nm with a variation of $V_{SIDE\ D,S}$ (1.0, 1.2, 1.5V).

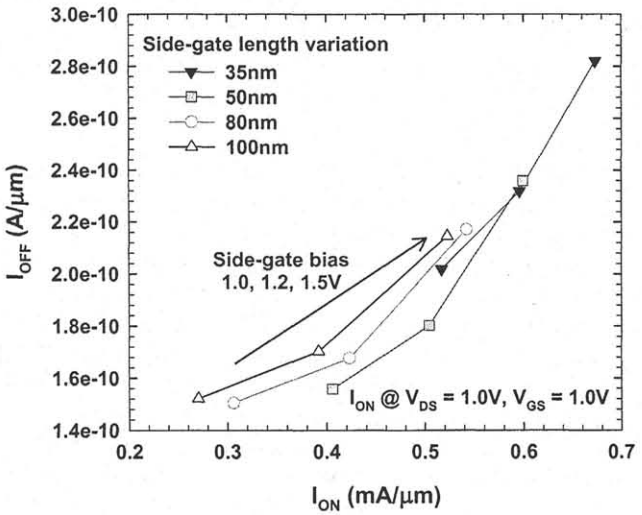

Fig. 4 I_{ON}-I_{OFF} characteristics with the variation of side-gate length. I_{ON} is drain currents that measured at V_{DS}=1.0V.

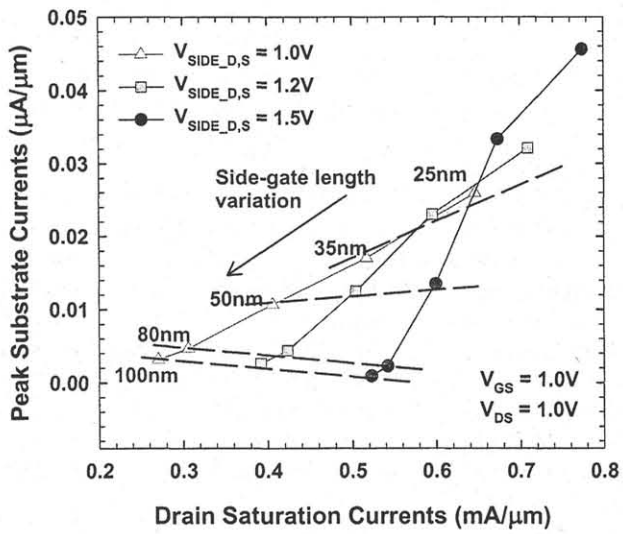

Fig. 5 Simulated side-gate MOSFET peak substrate currents vs. drain saturation currents.