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A Fully Monolithic Integrated 43-Gbit/s Clock and Data Recovery Circuit Using InAlAs/InGaAs/InP HEMTs

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1. Introduction

There is strong demand for an expansion of transmission capacity due to the rapid growth of the Internet. A wavelength division multiplexing (WDM) system based on 40-Gbit/s class electrical time division multiplexing (ETDM) is a promising way to meet the requirements. The clock and data recovery circuit (CDR) is a key electronic component, and its fully monolithic integration is very attractive for reducing the size and power dissipation of the optical receivers. Up to now, 40-Gbit/s class monolithic integrated CDRs have been demonstrated by using Si-Ge bipolar [1] and GaAs HEMT [2] technologies. These CDRs use a circuit architecture that regenerates the input data signal with the half-rate clock signal. A 40-Gbit/s class monolithic CDR that operates with the data-rate clock signal has not been reported because of the difficulty in achieving high-speed circuit operation.

This paper describes a fully monolithic integrated 43-Gbit/s CDR that operates with the data-rate clock signal. The CDR is based on a PLL, and all components were monolithically fabricated with 0.1-μm gate-length InAlAs/InGaAs/InP HEMTs. Error-free operation of the fabricated IC was confirmed at 43.0184 Gbit/s, the data rate of optical channel transport unit 3 (OTU-3) [3]. To the best of our knowledge, this is the first demonstration of a fully monolithic 43-Gbit/s CDR IC operating with the recovered 43-GHz clock signal.

2. Circuit Configuration

The circuit block diagram of the CDR is shown in Fig. 1. The circuit architecture of the CDR is consistent with that in [4]. The circuit is based on an analog PLL that consists of a D-type flip-flop (D-FF), a phase comparator (PC), a 90-degree delay, a voltage-controlled oscillator (VCO), and a low pass filter (LPF). Incorporating the reference 90-degree delay into a conventional PLL enables both the recovered clock frequency and the phase timing to be adjusted automatically for the input data. In addition, a phase comparator circuit configuration that combines two multiplier circuits improves the tolerance for the data signal mark ratio variation [4, 5]. This PLL structure is expected to achieve high-speed and stable operation. The circuit was designed in the source coupled FET logic (SCFL), and the internal circuit operation is differential type. The CDR has a single-ended data input, a single-ended clock signal output, and a differential data output. The D-FF regenerates the input data signal using the output of the 43-GHz VCO.

Except for the phase comparator, the components in the CDR have different circuit configurations from those in [4]. The data buffer consists of three-stage differential amplifiers. A super-dynamic D-FF [6] was used as a core D-FF to achieve 43-Gbit/s operation with a sufficient speed margin. The 90-degree delay circuit is composed of two-stage differential amplifiers. The simulated gate-delay time is around 12 ps, which corresponds to the half-bit of the 43-Gbit/s non-return-to-zero (NRZ) input data signal. A lag-lead-type circuit consisting of an on-chip MIM capacitor and two on-chip metal resistors was used as the LPF. In order to realize a compact, low-noise oscillator, a differential amplifier with tuned tank circuits was adopted as the VCO [7]. The VCO circuit configuration is shown in Fig. 2. The inductors were formed with the second Au metal layer. Reverse-biased drain-source-shortened FETs were used for the varactors. The control voltage is input to the common gate of the FETs. The data output buffer consists of two-stage differential amplifiers and an open-drain-type driver. The clock output buffer is composed of two-stage inductor peaking amplifiers and an open-drain-type driver.

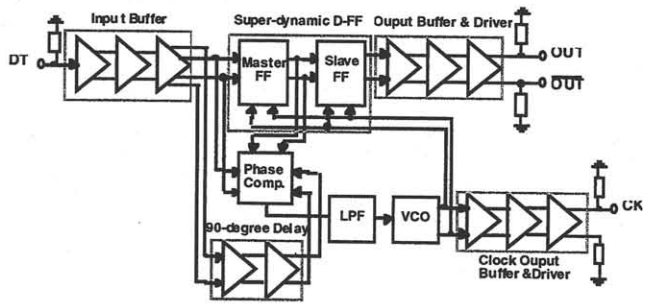


Fig. 1 Circuit block diagram of the CDR.

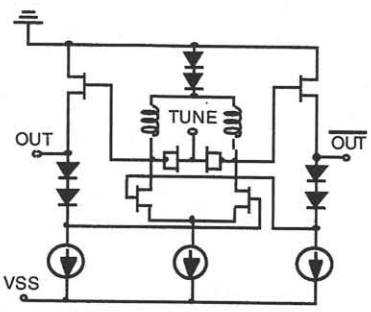


Fig. 2 Circuit configuration of the VCO.

3. Experimental Results

The CDR was fabricated with 0.1-μm gate-length InAlAs/InGaAs/InP HEMTs [8]. The averaged threshold voltage was – 543 mV with a standard deviation of 27 mV in a 3-inch wafer. The averaged transconductance was 1.23 S/mm, and the current gain cut-off frequency was 173 GHz. A photograph of the fabricated IC is shown in Fig. 3. The chip size is 3 mm x 2 mm.

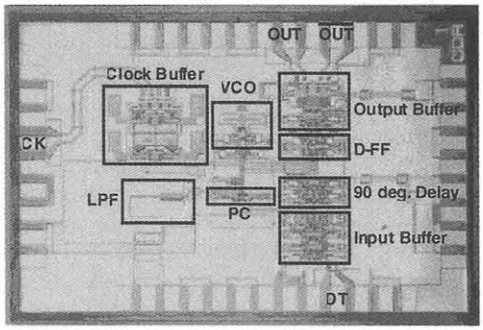
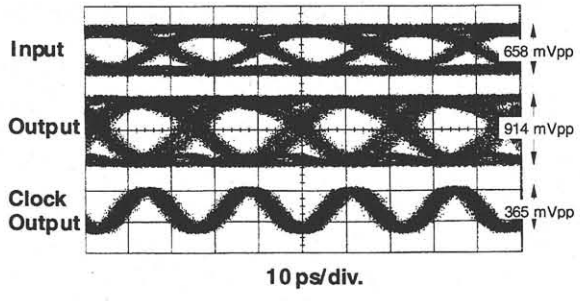


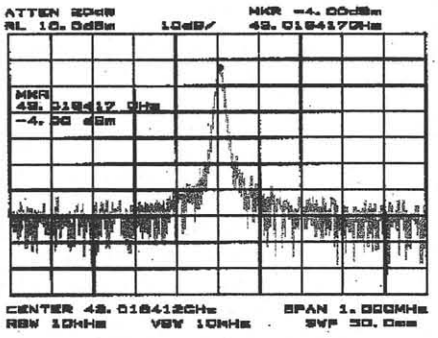
Fig. 3 Chip photograph of the CDR IC.

The IC was tested in on-wafer measurements. The input 43-Gbit/s NRZ signal was generated by the combination of a 4-ch. pulse pattern generator (PPG), a multiplexer unit, and an InP HEMT multiplexer IC module [9]. Since the PPG outputs four parallel pseudo random bit sequence (PRBS) signals while maintaining a quarter phase delay between each signal, the multiplexed 43-Gbit/s signal is truly PRBS signal. The output data signal of the CDR was demultiplexed twice using an InP HEMT decision IC module [9], and then input to an error detector. The recovered clock signal was monitored by a spectrum analyzer and/or a digitizing sampling oscilloscope synthesized with the PPG.

Figure 4(a) shows the operating waveforms of the CDR at 43.0184 Gbit/s. Figure 4(b) shows the spectrum of the recovered clock signal that was monitored via 1.3-m coaxial cable (~4 dB loss). Clear eye opening was observed with 914 mVp-p output voltage swing. Error-free operation was confirmed for the 2^{31}-1 PRBS data input. Recovered clock signal has a high signal-to-noise ratio of around 40 dB. The RMS jitter of the clock signal measured by the oscilloscope was only 1.2 ps. The power dissipation of the IC was 2.79 W.



(a)



(b)

Fig. 4 Operating waveforms of the CDR IC at 43.0184 Gbit/s.
(a) Input and output waveforms
(b) Spectrum of the recovered clock signal

4. Conclusions

We described a fully monolithic integrated 43-Gbit/s CDR for optical fiber communication systems. The PLL based CDR operates with the data-rate clock signal. The CDR was fabricated with 0.1-μm gate-length InAlAs/InGaA/InP HEMTs, and error-free operation was confirmed for 2^{31}-1 PRBS data signal at the OTU-3 bit rate of 43.0184 Gbit/s.

Acknowledgments

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