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A Noble Capacitive-Peaking Transimpedance Amplifier with High Linearity Gain Active Feedback Design

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1.Introduction

Transimpedance amplifiers (TIA), which are widely used for front-end receiver in optical communication syatems, can convert the optical signals into electrical signals. A TIA commonly consists of an inverter circuit, a resistive feedback (FB) loop, and an output impedance-matching buffer stage. The conventional FB-loop uses a passive resistor[1]. An active FB-resistor use a common-gate FET (CG-FET) has been designed by several groups [2]. This CG-FET FB-loop has several advantages over a resistor loop, such as, smaller overall chip size, tunable transimpedance gains (Z_Ts), and easier fabrication process. However, using that approach usually gives poor gain linearity, as compared with a FB-resistor. Gain linearity is an essential issue for amplifier operation, which determines the output signals modified by the controlling terminal. To overcome this drawback, we use a gate-source connected FET (GS-FET) as a FB-loop in this study. Owing to a better linearity by GS-FET feedback design, TIA exhibit a large ΔV_{out} at a small input current.

In addition, high-speed optoelectronic receivers (i.e., high speed TIAs) are required of very large capacity optical transmission systems. Many early research groups have been successful in designing and fabricating the high speed TIAs to be pre-amplifiers of photoreceivers[1]-[2]. To increase the bandwidth of TIA by reducing the gate-length of devices is a straightforward choice, but it increases the difficulties in fabrication process. Therefore, to boost the speed of TIA in optical communication systems is still in the research stage. One way to improve the bandwidth of TIA is called peaking technique, which usually places inductors (L-peaking) in a strategic location in TIA circuit, and therefore resulting in a resonance with parasitic capacitances and broaden the bandwidth of the amplifier[3]. Here, we propose a capacitive-peaking (C-peaking) technique, instead of an L-peaking, to increase the bandwidth of TIA without sacrificing its low-frequency gain. The C-peaking used in our study is to design a Butterworth-type TIA by adding an extra pole in amplifier circuit[4]. When the poles are complex conjugates with each other, the bandwidth of TIA is broadened. In addition, the size of a peaking capacitor (C_p) is relatively smaller than an inductor, and the parasitic effect can be reduced.

2. Circuit Design

Our TIAs were fabricated by using GaAs buried-channel MESFET structures, consisting of a 100nm thick-channel ($n = 2 \times 10^{17} cm^{-3}$) on the top and a 15nm thin-channel ($n = 1 \times 10^{18} cm^{-3}$) on the bottom. The schematic of GS-FET C-peaking TIA circuit is illustrated in Fig. 1. The blocks inside Fig. 1 show two configurations in the active feedback loop design, i.e. a CG-FET feedback,

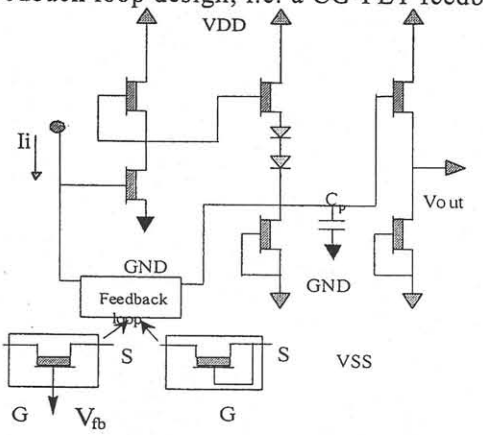

Fig. 1 The diagram of active-feedback C-peaking TIA and a GS-FET feedback, respectively. The gate for each individual device of TIA is 1.0μm long. In addition to the 1.0μm-long GS-FET, we also include 2.5 and 4μm ones to achieve different DC gains. Fig. 2 shows the DC I-V characteristics of MESFET. The dashed curve 1, 2 illustrate the I-V characteristics of CG-FET at V_{fb}=0V and -0.7V, respectively. The curve 3 represents the characteristics of GS-FET FB design. It is found that the

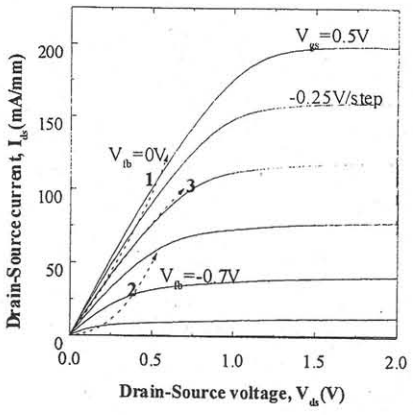

Fig. 2 Ids-Vgs of MESFET, where the dashed curves indicate the characteristics of feedback FET

effective channel resistance of the CG-FET feedback decreases while the dashed curve 1 and curve 2 move up. This is due to the V_{out} of TIA will modify the V_{gs} of the feedback CG-FET and it causes a channel resistance decrease in feedback FETs.

3. TIA Performance

Fig. 3 shows the DC characteristics of the CG-FET feedback TIA. The gate-length of CG-FET is 2.5μm. The Z_Ts, i.e. the slope of I-V curves, become smaller in the high injected current regime. Since the source terminal of feedback FET is directly modulated by the output negative voltage, the increased ΔV_{out} by a higher injected current corresponds to a decrease of $|V_{gs}|$ in

feedback CG-FETs. The channel resistance under this circumstance is therefore reduced, resulting in an output gain reduction. It limits the linearity of TIAs with a lower dynamic operational range. The individual gain of the CG-

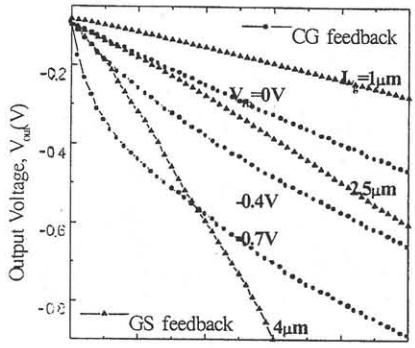

Fig.3 DC characteristics of the CG-FET and GS-FET TIA

feedback reductions shown in Fig. 3 are from 0.9kΩ to 0.65kΩ at V_{fb}=0V, from 1.8kΩ to 0.75kΩ at V_{fb}=-0.4V, from 5KΩ to 0.9KΩ at V_{fb}=-0.7V, respectively. Similar results were also observed in the previous reports[2]. The gain linearity of TIA can be improved by a GS-FET feedback design. Since the channel resistance of feedback FET remain a constant, the gain linearity is therefore improved. Fig.3 also shows the Z_Ts with a GS-FET feedback are 0.4kΩ, 0.9kΩ, and 2.4kΩ, corresponding to the feedback FET with a gate-length of 1, 2.5, and 4μm, respectively. The gain profiles present a better linearity than those in a CG-FET one, and this linear gain can still be obtained at a 500μA injected current.

Fig.4 shows the photograph of a GS-FET C-peaking

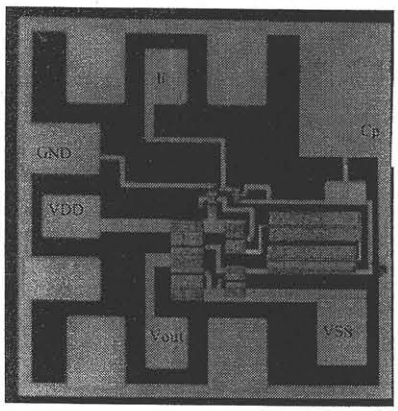

Fig.4 Photograph of GS-FET C-peaking TIA

TIA. Si_3N_4 films were deposited as an insulator of MIM capacitor and as a passivation layer. In receiver systems, this layer could also be the AR-coating layer of photo-detectors. Fig. 5 shows the SPICE simulation results with different C_p capacitances of TIA. The 3dB bandwidth obtained from simulation results based on the measured MESFETs model (1μm gate-length and 2.5μm at GS-FET) with a C-peaking design could be enhanced from 1.2GHz to 2.2GHz. By varying the capacitance of C_p, we can modify the magnitude of the peak gain and enhance the bandwidth of TIA without sacrificing the low-frequency

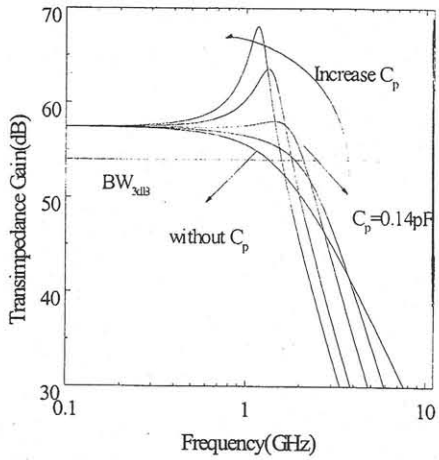

Fig. 5 Spice results with different Cps of C-peaking TIA

transimpedance gain. The DC gain of TIA under on wafer measurement almost remains the same before and after adding the C_p. This shows that the C_p will not affect the low-frequency transimpedance gain.

Fig. 6 shows the measured 3-dB bandwidth of TZ amplifier before and after adding the C_p. The 3-dB bandwidth of TIA without C_p is 1.1GHz for 2.5μm GS-FET, and 0.5GHz for 4μm GS-FET, respectively. These value can be referred as w_{3dB}, and make us to determine the proper value of C_p to achieve the Butterworth design, therefore, increasing the bandwidth of TIA. The optimum capacitance of C_p is 0.14pF from calculating the Butterworth design. After C_p is added in this circuit, the 3-dB bandwidth is enhanced from 1.1GHz to 2.3GHz, and 0.5GHz to 1.2GHz owing to the peaking effect, which is quite consistent with simulations.

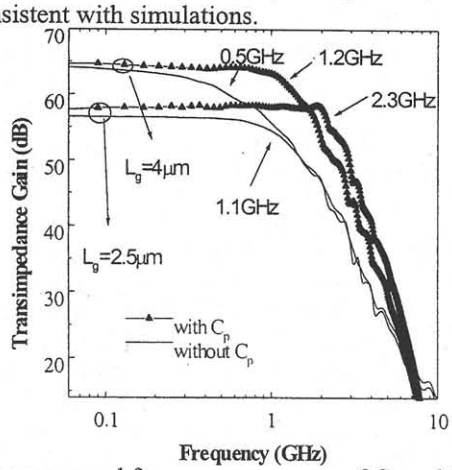

Fig. 6 The measured frequency response of C-peaking TIA

4. Conclusions

In this manuscript, we not only demonstrate TIAs with high linearity gain but show a C-peaking technique to broaden their bandwidth. This approach provides an easy way to enhance the bandwidth of optical receiving front-end, without further investing any sophisticated process equipments.

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