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Device Physics of Sub-100 nm Transistors

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Abstract

A new approach based on the transmission (or scattering) approach widely used for mesoscropic devices is applied to Si transistors. By examining a familiar device from a fresh perspective, new insights into the physics of nanoscale transistors and their ultimate limits are obtained.

1. Introduction

This talk presents a simple view of the physics of transistors with nanoscale dimensions. A theory for the ballistic MOSFET will first be presented and used to establish theoretical performance limits for transistors. The role of scattering, which limits the performance of actual devices will then be examined using a transmission theory similar to that used for conduction in mesoscopic and molecular scale structures. As channel lengths shrink, the transistor's on-current approaches an upper limit; present day devices operate with on-currents that are within ~50% of the ballistic limit. The MOSFET channel resistance also approaches a lower limit as L approaches zero (analogous to the e^2/h quantum contact resistance). Different types of devices (e.g. bulk or SOI) have different performance limits. The transmission view provides a clear, yet simple, picture of transistor physics at the nanoscale. It should prove useful for exploring ways to push transistors to their limits as well as serve as a jumping off point for exploring radically new approaches such as molecular devices.

2. The Transmission Approach to MOSFETs

Figure 1 summarizes the essential physical picture that will be discussed in this talk. Carriers are injected into the channel from a thermal equilibrium reservoir (the source), across a potential energy barrier whose height is modulated by the gate voltage, into the channel, which is defined to begin at the top of the barrier. The beginning of the channel is populated by carriers injected from the thermal equilibrium source (and, under low drain bias, from the thermal equilibrium drain as well). The density of carriers at the top of the barrier is controlled by MOS electrostatics so that the charge in the semiconductor balances that in the gate. Under equilibrium conditions (V_{DS} = 0V) in an electrostatically well-tempered device, equilibrium, 1D MOS electrostatics apply at this point, so the inversion layer density can be computed as for a 1D MOS capacitor. Numerical simulations show that a type of "gradual channel approximation" applies at this point, so that the inversion layer density at the source end of the channel remains nearly equal to its equilibrium value even when a drain bias is applied. From this approach, a very simple theory of the ballistic transistor, which gives the upper limit current for a MOSFET, can be developed [1-3].

Some fraction of the carriers injected from the source into the channel backscatter and return to the source; others flow out the drain and comprise the steady-state drain current, I_D. (For a high drain bias, carriers injected from the drain need not be considered.) Assuming current continuity, I_D may be evaluated at the beginning of the channel where the carrier density is known from MOS electrostatics to find [4]

$$I_D = WQ_i(0)\langle\upsilon(0)\rangle \approx W\left\{C_{ox}\left(V_{GS}-V_T\right)\right\}\left\{\left(\frac{1-r}{1+r}\right)\tilde{\upsilon}_T\right\},$$

where $\langle\upsilon(0)\rangle$ is the average velocity of carriers at the beginning of the channel. The maximum value of $\langle\upsilon(0)\rangle$ is approximately the equilibrium uni-directional thermal velocity, $\tilde{\upsilon}_T$, because the positive velocity carriers at the beginning of the channel were injected from the thermal equilibrium source. Backscattering from the channel determines how close to this upper limit the device operates. Under high drain bias, the average velocity at the beginning of the channel is related to a channel transmission coefficient, r, where $0 < r < 1$ is a backscattering coefficient in the spirit of McKelvey [5].

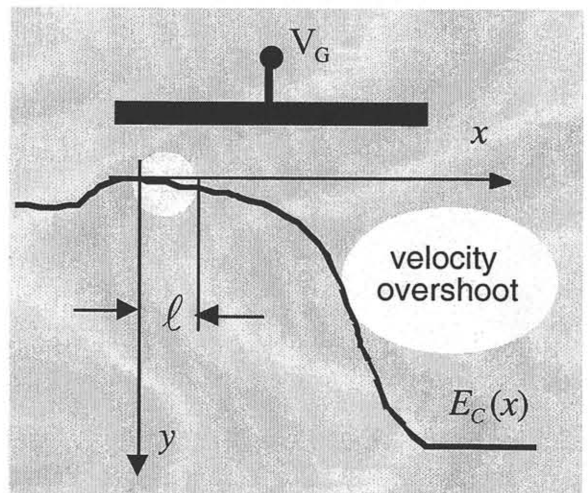

Fig. 1 The conduction subband edge *vs.* position from the source to the drain of a nanoscale MOSFET under high gate and drain bias. Also shown are the thermal injection fluxes from the source and drain and the critical region for carrier backscattering.

Because of the high electric field and strong velocity overshoot, carrier transport through the drain end of the channel is rapid. The D.C. current is controlled by how rapidly carriers are transported across a short low-field region near the beginning of the channel. We refer to the critical, low field region near the beginning of the channel as the "*kT*-layer" because it is roughly the distance over which the channel potential drops by k_BT/q. Scattering within the *kT*-layer limits the steady-state drain current by reducing r, while scattering near the drain end of the channel has only an indirect effect on r. This is analogous to the well-known Bethe condition for thermionic emission in a forward-biased metal-semiconductor diode, except that in a MOSFET the flow of carriers is down the potential barrier rather than up.

3. Discussion

The basic, physical picture in Sec. 2 will be developed and illustrated by numerical simulations. Using this approach, several issues will be examined:

1) injection velocity limits at the source end of the channel
2) the off-equilibrium distribution function at the source
3) charge control in a nanoscale MOSFET
4) the role of scattering and the generalized Bethe condition for a MOSFET
5) the role of velocity overshoot in the channel
6) the magnitude of the quantum contact resistance in nanoscale MOSFETs
7) the expected performance of end-of-the-Roadmap MOSFETs
8) why traditional models provide such a good guide to device design,
9) when traditional models will fail,
10) how one should interpret results of detailed simulations and
11) what this new view has to say about the future evolution of CMOS device technology.

A key insight from the transmission approach is that there exists a maximum source velocity – no matter how short the channel is or how strong the resulting velocity overshoot is. This thermal injection velocity limit depends on how the subband are occupied and on the degree of carrier degeneracy. Its typical value is roughly 1.5 x 10^7 cm/s. Although this velocity exceeds the saturated velocity, it represents the thermal velocity of an *equilibrium* hemi-Fermi-Dirac distribution and has nothing to do with the velocity overshoot that occurs when the electric filed changes rapidly.

Of course, strong velocity overshoot does occur within the channel of a nanoscale MOSFET. The high source velocity limit due to thermal injection cannot be observed unless the velocity in the rest of the channel is even higher. Velocity overshoot within the channel affects the change density within the channel, and, therfore, through Poisson's equation, the electric field near the source. The effect of velocity overshoot within the channel may be strong, be it is an indirect one.

An interesting insight from the transmission approach is that the near-equilibrium mobility continues to be a relevant parameter – even in nanoscale MOSFETs. The reason is that the backscattering that limits the steady-state current occurs very near the source, before carrier are significantly heated. The backscattering coefficient, r, is determined by the near-equilibrium mean-free-path, which is related to the mobility. Techniques to improve carrier mobility, such as the use of strain, should, therefore, continue to improve the on-current of a nanoscale MOSFET.

Finally, it is interesting that a well-designed MOSFET appears to have a backscattering coefficient of roughly 50% - independent of technology node. This occurs because as the channel length shrinks, which reduces, r, the channel doping increases and the oxide thickness decreases, both of which increase r. The result is that r is approximately constant, so bulk CMOS transistors will continue to operate at ~50% of the ballistic limit as long as they are scaled. Other device architectures, however, (such as fully-depleted SOI) could operate closer to the ballistic limit.

4. Conclusions

In summary, we present a new view of nanoscale silicon MOSFETS that provides a new perspective on the device. Note that although the focus of this paper is on MOSFETs, similar concepts apply to bipolar transistors as well [6]. The approach is fully consistent with traditional methods of modeling transistors, but it should also prove applicable to the new kinds of devices that may follow CMOS transistors.

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