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Experimental Evidence of Inversion-Layer Mobility Lowering in Ultrathin Gate Oxide MOSFETs with Direct Tunneling Current

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1. Introduction

Low field mobility is still one of the most important device parameters for scaled MOSFETs. It has recently been reported that MOSFETs with ultrathin gate oxides allowing significant direct tunneling current can exhibit lower inversion-layer mobility, because of several plausible scattering mechanisms inherent to ultrathin gate oxides, such as remote impurity scattering [1-3], poly Si/SiO_2 interface roughness scattering [4] and MOS interface plasmon scattering [5]. Actually, the decrease in G_m with a decrease in gate oxide thickness, T_{ox}, has been observed in T_{ox} region down to 1.5 nm [6]. However, the direct experimental evidence of mobility lowering with ultrathin gate oxides less than 3 nm has not been sufficient yet. This lack in the experimental result is attributable to the fact that high gate current prevents us from simply using the conventional split C-V method for mobility extraction.

This paper shows that, by modifying split C-V method under optimized device size and measurement parameters, inversion-layer mobility of MOSFETs with ultrathin gate oxides can be accurately determined, at least down to T_{ox} of 1.5 nm. It is experimentally shown, as a consequence, that mobility decreases in lower E_{eff} or N_s (surface carrier concentration) region with a decrease in T_{ox}, while little lowering of mobility is observed in higher E_{eff} or N_s region.

2. Measurement Method and Samples

There are mainly two difficulties in the mobility measurement for MOSFETs with high gate current. One is that the channel conductance cannot be determined simply by the derivative of I_D with respect to V_D, as shown in Fig. 1 and Fig. 2. However, if source and drain regions are symmetry for gate electrode and V_D is sufficiently small, the current from the source to the gate and the current from the drain to the gate must be identical. Therefore, the drain conductance, G_D, is determined by the derivative of $(I_D-I_S)/2V_D$ with respect to V_D. No V_D dependence of G_D, shown in Fig. 2, validates the accuracy of measured G_D.

The other difficulty in mobility measurement is that C_{gc}-V_G measurement becomes inaccurate for T_{ox} with higher leakage current, because of the significant influence of the channel resistance [7]. However, this problem is avoidable by using MOSFETs with relatively short gate length, which reduce the channel resistance. On the other hand, the gate length should be long enough to define the channel length. Fig. 3 shows C_{gc}-V_G curves for L/W of 10 μm/10 μm as a parameter of measurement frequency. Almost no frequency dependence and the good agreement with C_{gc} determined by the two-frequency method [7] validate the accuracy of C_{gc} measurement. As a result, inversion-layer mobility can be determined by combining the above measurements of G_D and $C_{gc}(N_s)$ under the framework of the split C-V method.

N-channel MOSFETs used in the measurement have gate oxides of pure SiO_2 with T_{ox} of 3.5, 2.8, 2.2 and 1.5 nm for comparison with the universal mobility [8]. The substrate impurity concentration has been chosen to be as low as 2-3 $\times10^{16}$ cm^{-3} in order to reduce the influence of substrate impurity scattering. It has been confirmed from C-V characteristics that there is no significant penetration of As atoms in the poly-Si gate into substrates.

3. Experimental Results

Fig. 4 shows the experimental mobility with T_{ox} of 3.5-1.5 nm and the universal mobility, as a function of E_{eff}. It is found that the mobility with T_{ox} less than 2.8 nm decreases in low E_{eff} region with a decrease in T_{ox}, while the mobility in higher E_{eff} region is in agreement with the universal mobility, down to 1.5 nm. Since the influence of gate current on I-V characteristics is larger in higher V_G or E_{eff} region, this mobility lowering in low E_{eff} region is not attributed to any spurious effect due to gate current, but to some additional scattering mechanism inherent to thin gate oxides.

Fig. 5 shows the mobility component due to this additional scattering mechanism as function of N_s. Here, according to Matthiessen's rule, the universal mobility and mobility limited by substrate impurity scattering [8] have been subtracted from the total mobility shown in Fig. 4. The mobility component due to the additional scattering is found to be almost constant, irrespective of N_s, which is not necessarily in agreement with the results of the theoretical calculations for several scattering mechanisms inherent to thin oxides [1-5]. Fig. 6 shows the T_{ox} dependence of this mobility component and the theoretical mobility values limited by remote impurity scattering [1, 2] at N_s of 2.8 $\times10^{12}$ cm^{-3}. Although the experimental T_{ox} dependence is similar with those in the theoretical calculations of remote impurity scattering [1, 2], these calculated mobility values have large variation in the amount. Thus, it is difficult, at present, to judge whether remote impurity scattering is responsible or not for the observed mobility lowering. As a result, the scattering mechanisms inherent to thin gate oxides, reported so far [1-5], seem not to be able to sufficiently explain the present experimental results in terms of the N_s dependence and the amount of mobility. Further theoretical studies on scattering mechanisms are needed to identify the physical origin of the mobility lowering.

4. Conclusion

It was experimentally found that inversion-layer electron mobility in the T_{ox} region less than 3 nm decreases in lower N_s or E_{eff} region with a decrease in T_{ox}. This fact means the existence of some additional scattering mechanism associated with thinning gate oxides.

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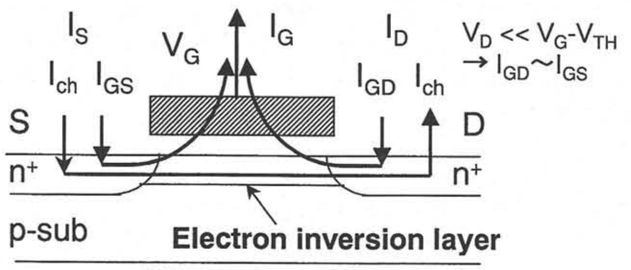

$$\mu(V_G)=\frac{L}{W}\boxed{\frac{(I_D(V_G)-I_S(V_G))}{2V_D}}\cdot\frac{1}{q\int_{-\infty}^{V_G}\left(C_{gc}(V_G')-C_{ov}\right)dV_G'}$$

Fig.1 Schematic diagram of current flow of MOSFETs with high gate tunneling current. Here, $I_S < 0$ and $I_D > 0$.

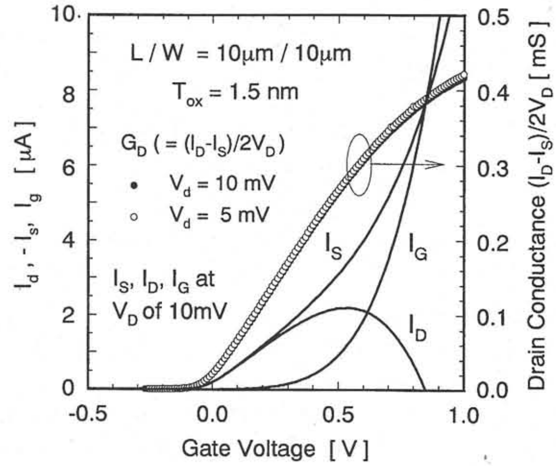

Fig.2 Drain, source and gate current (left axis) and drain conductance (right axis) as a function of V_G.

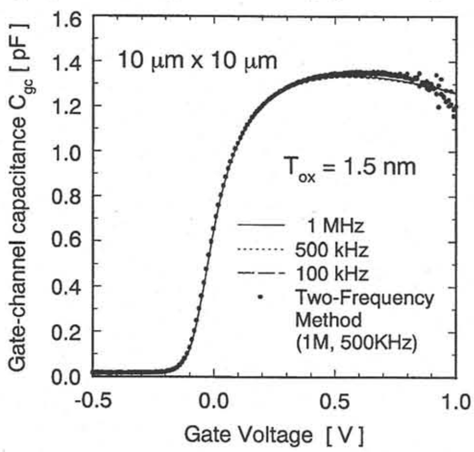

Fig.3 $C_{gc} - V_G$ characteristics of MOSFETs with L/W of 10 μm/10 μm and T_{ox} of 1.5 nm.

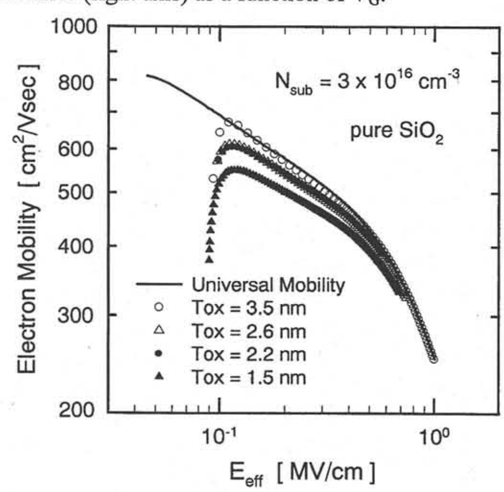

Fig.4 Inversion-layer electron mobility as a function of E_{eff} with T_{ox} of 3.5 – 1.5 nm. A solid line means the universal mobility

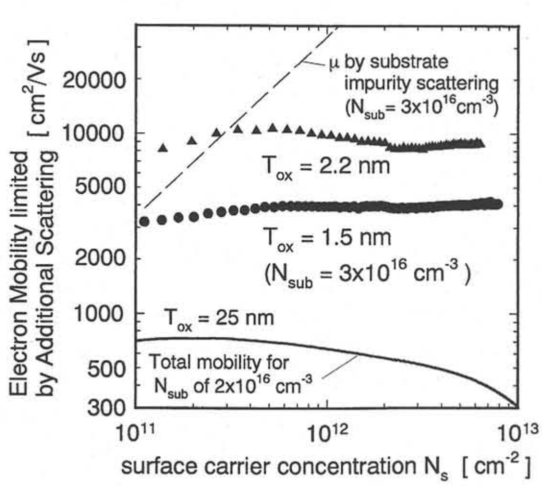

Fig.5 Mobility component of additional scattering mechanism, determined by Matthiessen's rule, as a function of N_s.

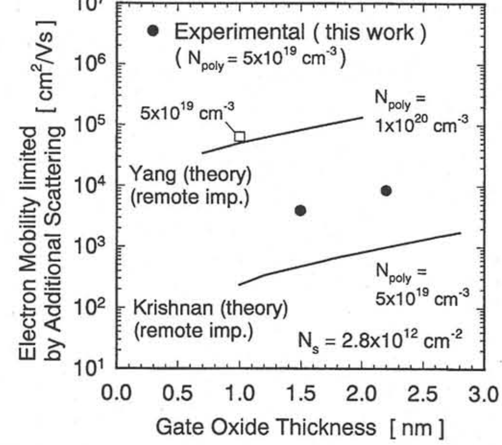

Fig.6 Mobility component of additional scattering term at N_s of 2.8 x10^{12} cm^{-3} as a function of T_{ox}. Solid lines show the calculated mobility by remote impurity scattering [1,2].