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High-Accuracy Analysis of Interconnect Capacitance for Floating Metal Fills

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1. Introduction

Floating electrodes, which are frequently sandwiched by signal lines, play essential roles in enhancing the planarization of interlayer dielectrics in the ULSI fabrication process (Fig. 1) [1][2]. These floating electrodes are called metal fills. The total capacitance is reduced by using floating metal fills rather than grounded metal fills.

To analyze the interconnect capacitance with high accuracy, we have developed a new method that combines conventional electrical field simulation and circuit simulation. In this method, the capacitance is obtained from the response time of a capacitance network calculated by electrical field simulation.

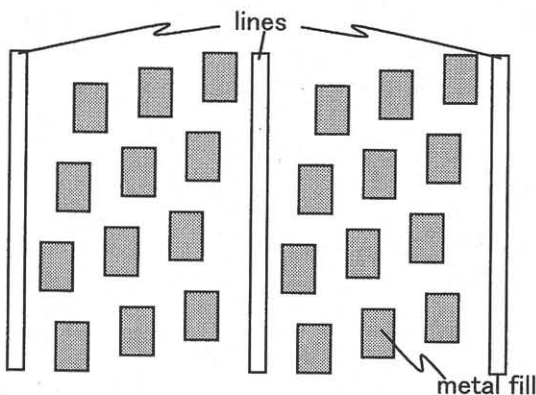


Fig. 1 Metal Fill Patterning

2. Effective Capacitance Extraction Method Using Decay Time Constant

The new method consists of three steps. The first step is to determine the electrical field distribution for electrically fixed electrodes, as well as capacitance value C and a capacitance network. We use an integrated Green's function method, called TRISIM1 [3], which works well for a large-scale structure. As a second step, we focus on two nodes for analyzing capacitance and insert a resistance R between these nodes. The capacitance and resistance circuit is then constructed (inset in Fig. 2). The last step is to obtain the decay time constant τ by circuit simulation and calculate the

effective capacitance $C_{eff} = \tau/R$ (Fig. 2). This method requires no difficult iterative calculations with convergence. Thus, we can achieve high-speed calculation with high accuracy by using the integrated Green's function method.

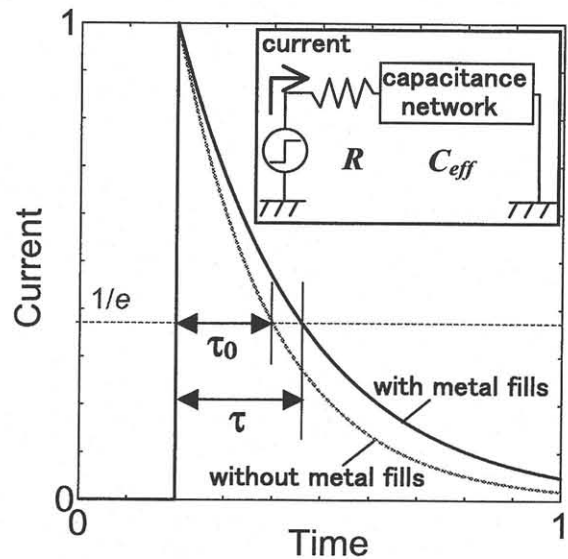


Fig. 2 Decay time constant τ

3. Result

We analyzed the capacitance (C/C_0) by inserting floating metal fills between electrically fixed lines, where C_0 and C are the capacitance values without and with metal fills, respectively. There are two major factors that determine the electrical field distribution. One is the area density of the metal fills, and the other is the aspect ratio of the metal fills. We investigated C/C_0 with respect to these two factors.

We analyzed C/C_0 as a function of the area density, which is defined as the occupation ratio of floating metal fills. We calculated C/C_0 for (5×5) structure of floating metal fills (inset in Fig. 3). As the area density increased, C/C_0 increased rapidly because the total area of dielectric decreased sharply (Fig. 3). When the area density was 0.2%, C/C_0 was 1.15. The deviation from unity arises from fringe components that break the uniformity of the electrical field distribution.

Next, we analyzed C/C_0 as a function of the aspect ratio (Fig. 4). In this analysis, we inserted a series of floating metal fills (inset in Fig. 4) and fixed the area density at 25.0%, which means the horizontal dimension of the metal fills was equal to the distance between fills, and the vertical dimension of the metal fills was equal to half the distance between electrically fixed lines. When the aspect ratio was unity, C/C_0 was 1.75 (Fig. 3).

As the length (a) of the metal fills is increased for vertical fills, C/C_0 is asymptotic to 2.00. This is because the field strength between metal fills weakens under the constant-area-density condition, and the field strength is then determined from the distance obtained by subtracting the distance from the width of the fills. On the other hand, as the length (a) of the metal fills is increased for horizontal fills, C/C_0 approaches 1.50. The capacitance is determined by the average value of the capacitances in two regions: one is a region where electric flux lines are terminated by metal fills; the other is a region where electric flux lines are terminated by electrically fixed lines. We should note that C/C_0 is more sensitive to aspect-ratio variation for vertical metal fills than for horizontal metal fills. Thus, when metal fills with the same rectangular structure are laid wall-to-wall on a chip, there is a tradeoff with respect to aspect ratio.

This method can thus provide exact quantitative capacitance values for ULSI design.

4. Conclusions

We have developed a new method for analyzing interconnect capacitance that combines conventional electrical field simulation and circuit simulation, and obtains the response time of a capacitance network. With this method, we can quantitatively analyze the capacitance of both symmetrical and asymmetrical geometries that include many floating electrodes. This method is thus a very useful ULSI design tool for obtaining exact 3-D capacitance.

Acknowledgments

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References

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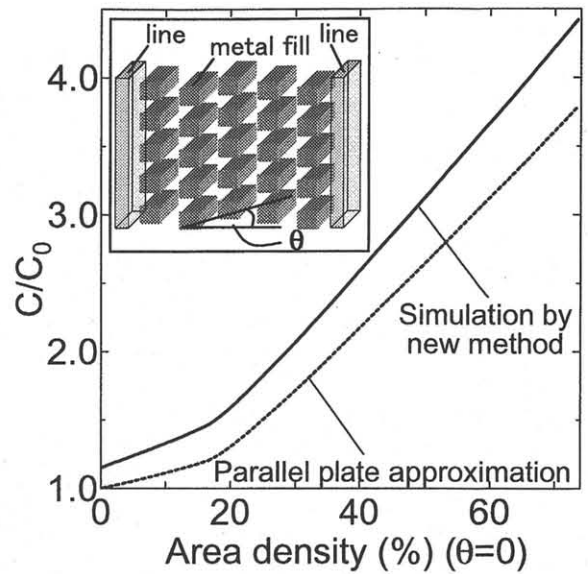


Fig. 3 Area density dependence

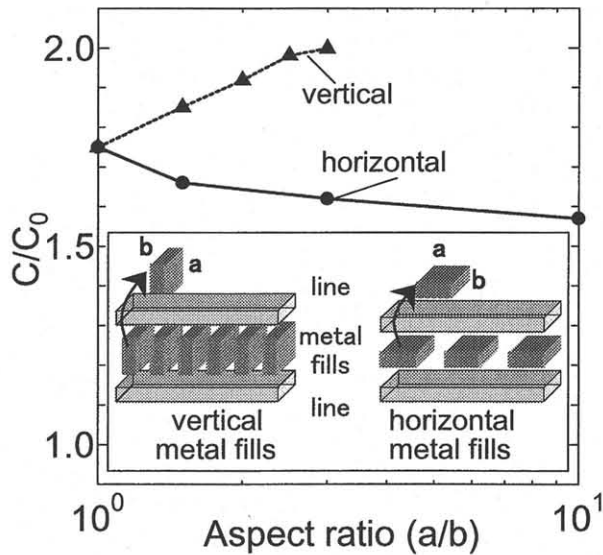


Fig. 4 Aspect ratio dependence