

**F-6-1 (Invited)****All-Polymer Thin Film Transistors Fabricated by High-Resolution Ink-jet Printing**Henning Sirringhaus, Takeo Kawase<sup>1</sup>, Tatsuya Shimoda<sup>1</sup>, and Richard Friend

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<sup>1</sup>Epson Cambridge Laboratory, 8c King's Parade, Cambridge, CB2 1SJ**1. Introduction**

Conjugated polymer semiconductors deposited from solution are best known for their electroluminescent properties and use in light-emitting diode devices. However, they have recently also become of interest for applications in thin film transistors. By making use of self-organisation mechanisms such as phase separation or liquid crystallinity ordered thin films can be deposited from solution in which high charge carrier mobilities on the order  $10^{-2}$ – $10^{-1}$   $\text{cm}^2/\text{Vs}$  can be achieved. In contrast to inorganic semiconductor transistors which are fabricated by complex vacuum deposition and photolithography, polymer semiconductors may enable low-cost fabrication of functional transistor circuits by a combination of solution processing and direct printing.

**2. Results**

We have developed a process by which complete polymer transistor circuits can be fabricated by direct ink-jet printing [1]. This process illustrates the potential of being able to control the solution deposition and structure of polymers on a microscopic and mesoscopic scale in order to fabricate functional, ordered device structures.

One of its key features is the ability to print with a high resolution of 5  $\mu\text{m}$ , which is required to define the small, critical gap between the source and drain electrodes of a transistor. This high resolution is achieved by confining spreading of water-based conducting polymer ink droplets of PEDOT/PSS on a hydrophilic substrate with a pattern of narrow, hydrophobic surface regions that define the critical device dimension, the channel length  $L$  (Fig. 1). After inkjet printing of source-drain electrodes, TFT devices are fabricated in a top-gate configuration by spin coating continuous films of the active semiconducting polymer and a polymer gate dielectric, and finally ink-jet printing a PEDOT/PSS gate electrode registered accurately with the underlying channel region. For the semiconducting polymer we use liquid-crystalline polyfluorene block copolymers the chains of which are uniaxially aligned parallel to the transport direction in the transistor. In this way we have demonstrated all-polymer, inkjet printed TFT with high

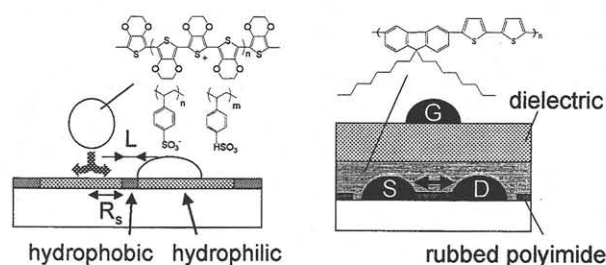


Fig. 1: Schematic illustration of (left) high-resolution ink-jet printing of conducting PEDOT/PSS onto a prepatterned substrate with a hydrophobic polyimide (PI) bank and (right) completed top gate (G) transistor devices with ink-jet printed PEDOT/PSS source-drain (S/D), a PVP gate dielectric and a polyfluorene block copolymer active semiconducting layer.

mobility of  $2 \cdot 10^{-2}$   $\text{cm}^2/\text{Vs}$ , high ON-OFF current ratio of  $10^5$ , and good operating stability.

To fabricate complex integrated transistor circuits by inkjet printing, circuit components other than TFTs are required as well. Of particular importance are via-hole interconnects, which provide electrical connections between electrodes and/or interconnects in different layers. We have developed an inkjet printing process for integrated via-hole fabrication. It is based on the local dissolution of materials by ink-jet deposition of a good solvent. To fabricate a via-hole through a layer of dielectric, for example, a droplet of a good solvent is deposited locally. The dielectric material locally dissolves and upon drying of the solvent redeposits on the side walls of a crater-like intrusion. This is repeated several times until the surface of the underlying layer, which also provides an automatic "etch stop", is exposed. Via-holes are filled by printing of PEDOT/PSS. The mechanism for via-hole formation is similar to that of the familiar coffee-stain, where during drying material is transported to the edge of the droplet, and no material redeposition occurs in the center of the droplet.

Printing processes for other components such as resistors and capacitors have been developed as well. This provides us

with all the basic building blocks to demonstrate functional logic circuits fabricated by ink-jet printing. Fig. 2 shows a photograph and characteristics of all polymer inkjet printed inverter circuits.

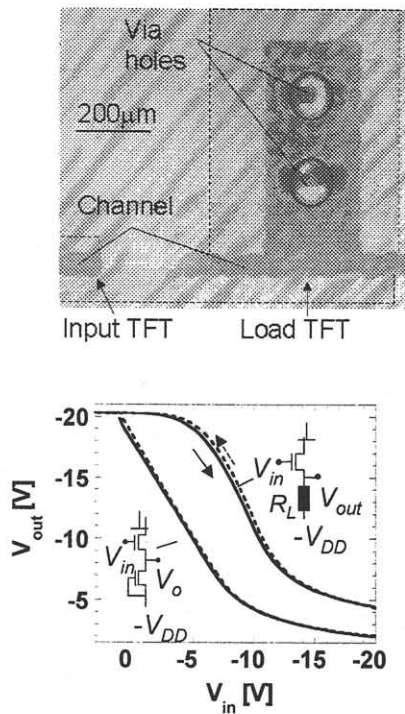


Fig. 2 Photograph (top) and characteristics (bottom) of inkjet printed all-polymer inverter circuits.

### 3. Conclusions

We have shown that solution self-assembly and direct inkjet printing techniques allow the controlled fabrication of high-mobility, short-channel ( $5\mu\text{m}$ ) polymer transistors and complete transistor circuits including via-hole interconnects. The device performance of printed polymer TFTs with mobilities up to  $2 \cdot 10^{-2} \text{ cm}^2/\text{Vs}$  and ON-OFF current switching ratios of  $10^5$  is believed to be adequate for practical applications in active matrix display addressing or logic circuits in identification tags.

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### References

- [1] H. Sirringhaus et al., *Science* 290 (2000) , p. 2123.