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Direct Growth of Single Crystalline CeO_2 High-k Gate Dielectrics

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1. Introduction

Epitaxial single crystalline high-k dielectrics directly grown on Si, which enable further reduction of equivalent oxide thickness (EOT), would be a potential candidate for a gate oxide in the 40nm CMOS technology. As it is well known that elimination of an amorphous interfacial layer is difficult, there are quite few reports on direct growth of high-k oxides on Si. Although McKee et al. reported direct growth of $SrTiO_3$ on Si and FET operation using $SrTiO_3$/Si as gate oxide [1], ability of single crystalline oxide directly grown on Si is still unclear.

CeO_2 is considered to be a good alternative dielectric for the Si-based devices due its good lattice matching with Si(Δd=-0.35%) and stable chemical properties. Previous studies indicate that Si (111) substrates are necessary for growth of single crystalline CeO_2 [2]. In this paper, we have successfully grown epitaxial CeO_2 directly on Si (111) and demonstrated a 5nm-thick CeO_2 MIS capacitor with EOT=0.38nm. We believe single crystalline CeO_2 has high potential as an alternative gate oxide.

2. Experiment

CeO_2 was grown on p-Si(111) substrates by molecular beam epitaxy (MBE) using metal Ce and O_3 as source materials. To avoid the formation of an amorphous interfacial layer, 0.6 monolayer of Ce was deposited on Si prior to O_3 supply. Physical thickness (T_{phys}) of CeO_2 were 5nm and 10nm. MIS capacitors were fabricated by evaporating Au using metal masks.

3. Results and discussions

Figure 1 shows the Rheed pattern of CeO_2 grown at 700℃. Sharp streak patterns indicate a flat surface of epitaxial CeO_2. A cross-sectional TEM image of the CeO_2/Si(111) interface is shown in Fig.2. It can be seen that CeO_2 was directly grown on Si without any interfacial layer. An atomic step is also clearly observed.

We have proposed a new method to construct "ideal" CV curves for ultra-thin gate dielectrics taking account of quantum mechanical effects in a Si substrate [3]. As shown in Fig.3, "ideal" CV curves (re-constructed from the experimental CV data of a SiO_2(3.5nm)/Si(111) capacitor) show good agreements with CV data of CeO_2/Si(111) capacitors, which were obtained by the two frequency CV method (f=200kHz and 1MHz) [4]. No hysteresis was observed in the CV measurements. EOT of CeO_2 epitaxial layers (T_{phys} = 5nm and 10nm) were estimated to be 0.38nm and 0.75nm, respectively. EOT has a good linear relation with T_{phys} as shown in Fig.4. The dielectric constant (ε) is ~52, calculated from the slope. This value is twice as large as the reported value of bulk (polycrystalline) CeO_2 (ε~26). This large value would be due to anisotropy of ε in single crystalline and/or lattice distortion of CeO_2 on Si.

We have performed the conductance method [5] to determine D_{it}. Figure.5 shows the equivalent parallel conductance (G_p) of the CeO_2 MIS capacitor (T_{phys} =10nm) as a function of measurement frequency (f). No post annealing process was performed to the capacitor. D_{it} is obtained to be $1.2 \times 10^{13}cm^{-2}eV^{-1}$ from the maximum G_p/ω at f=200kHz ($D_{it}=2(G_p/\omega)_{max}/q$). This D_{it} value is the same order as that of a Zr-silicate MIS capacitor without post annealing [3]. Further reduction of D_{it} will be investigated.

Figure 6 shows the relationship between EOT and leakage current density (J) at an equivalent electrical field of 5 MV/cm for a CeO_2 MIS capacitor (T_{phys}=5nm), compared with SiO_2 MIS capacitors [6]. J (0.9A/cm^2) for the CeO_2 capacitor (EOT=0.38nm) is six orders of magnitude lower than the expected J for SiO_2 capacitors with the same EOT.

4. Conclusions

We have grown CeO_2 directly on Si (111) by MBE. EOT as low as 0.38nm and high ε (~52) were obtained by elimination of an interfacial layer and single crystalline properties of CeO_2. We revealed that single crystalline CeO_2 directly grown on Si really works as gate dielectrics.

Acknowledgements

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References

[1] R. A. McKee, F. J. Walker and M. F. Chisholm, Science **293**, 468 (2001).

[2] M. Yoshimoto, K. Shimozono, T. Maeda, T. Ohnishi, M. Kumagai, T. Chikyow, O. Ishiyama, M. Shinohara and H. Koinuma, Jpn. J. Appl. Phys. **34**, L686 (1995).

[3] N. Yasuda and H. Satake, to be published in *Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, 2001.*

[4] A. Nara, N. Yasuda, H. Satake and A. Toriumi, *Extended Abstracts of the 2000 International Conference on Solid State Devices and Materials, 2000* (2000) p. 452.

[5] D. K. Schroder, "Semiconductor Material and Device Characterization", John Wiley & Sons, Inc. (1990).

[6] M. Hirose, M. Koh, W. Misubayashi, H. Murakami, K. Shibahara and S. Miyazaki, Semicond. Sci. Technol. **15**, 485 (2000).

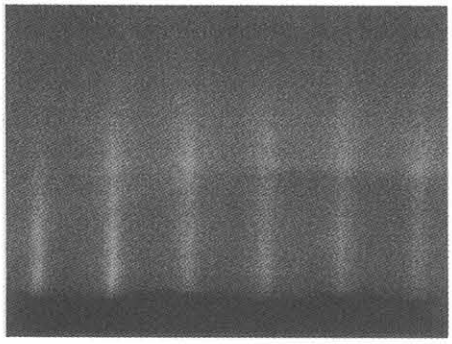

Fig.1 Rheed pattern along the <211> azimuth after growth of 10nm CeO_2 on Si (111) at 700℃.

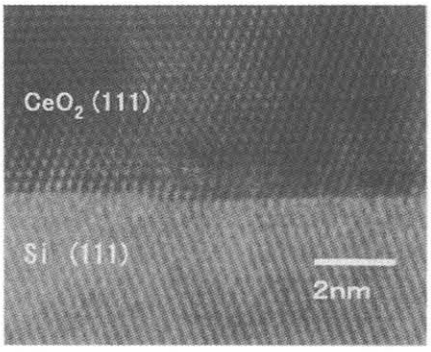

Fig.2 A cross-sectional TEM image of CeO_2 / Si (111) interface without any amorphous layer.

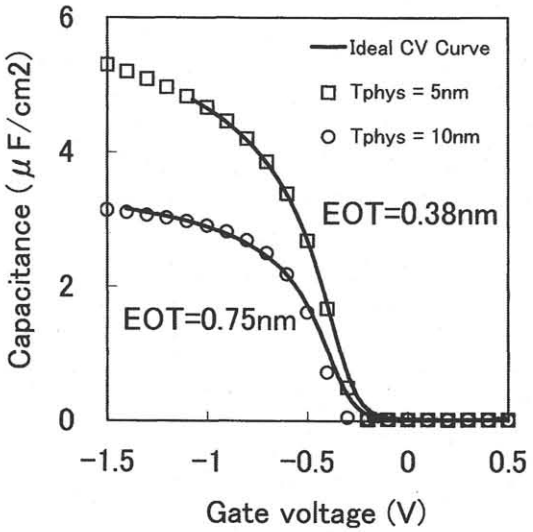

Fig.3 CV data of CeO_2 MIS capacitors (T_{phys}=5, 10 nm) and the "ideal" CV curves for EOT=0.38 and 0.75 nm constructed by a new method.

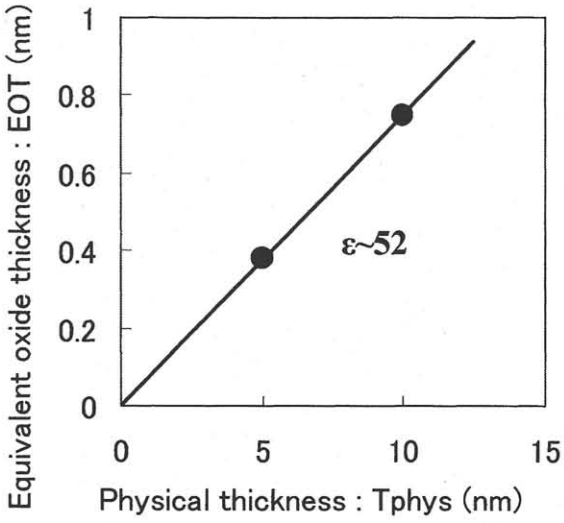

Fig.4 T_{phys} vs. EOT for CeO_2 MIS capacitors. The dielectric constant (ε) is calculated to be ~52 from the linear slope.

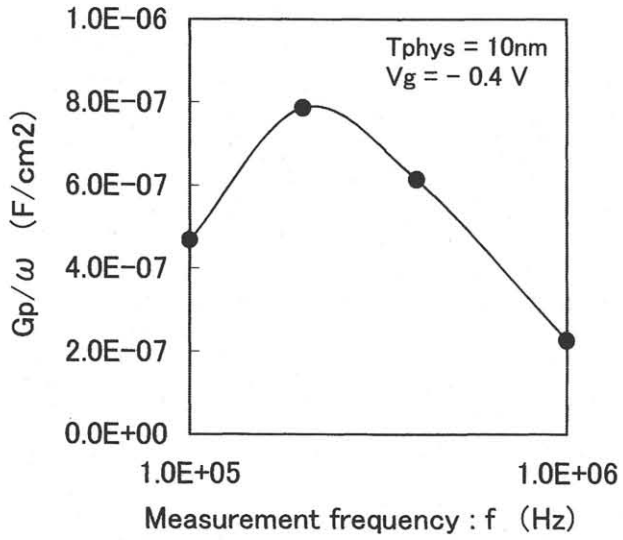

Fig.5 The equivalent parallel conductance (G_p) as a function of measurement frequency (f). D_{it} is estimated to be $1.2 \times 10^{13} cm^{-2} eV^{-1}$.

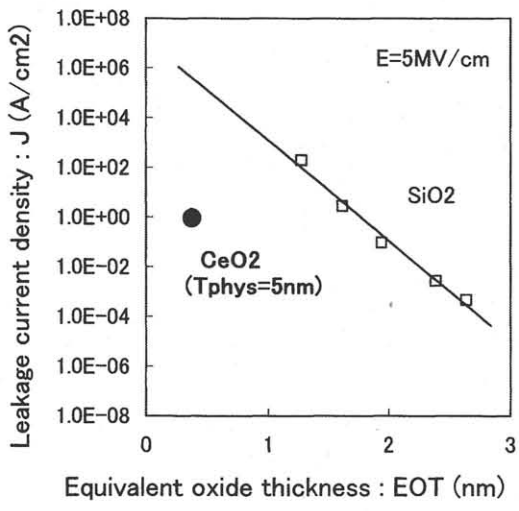

Fig.6 Relationship between EOT and J at E=5MV/cm for a CeO_2 (T_{phys}=5nm) and SiO_2 MIS capacitors [6].