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Micro Bump Interconnection Technologies in 20 μm Pitch on 3D System in Package

Tadahiro Morifuji, Yoshihiro Tomita, Ryoichi Kajiwara, Kenji Takahashi

Association of Super-Advanced Electronics Technologies (ASET)
Electronic System Integration Technology Research Department, Tsukuba Research Center
Room C-B-5, Tsukuba Center Inc., 1-6, Sengen 2-chome, Tsukuba, Ibaraki 305-0047, JAPAN
Phone: +81-298-60-2400 / Fax: +81-298-58-6177 / E-mail: morifuji@si3d-aset-unet.ocn.ne.jp

1. Introduction

Nowadays, the demand for the high-density electronics component is quite general for the consumer information equipment. The new packaging technologies are required to break through the limitation of the conventional package performance [1]. 3-Dimensional (3D) chip stacking that realizes the shortest wiring length between the chips is one of the most important technologies. Figure 1 shows a cross-section of 3D LSI structure. The exposed electrodes are allocated in 20μm-pitch on the back surface of the each device. And the copper electrodes are formed through the Si devices in 50μm thickness.

The hyperfine flip-chip binding at low temperature and stress is a key technology to achieve the structure. In this paper, the hardness control for low stress and ultra-sonic flip-chip bonding (UFB) for low temperature are described.

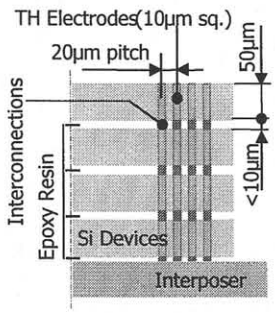


Fig. 1 3D LSI Structure

2. Experiment

Figure 2(a) and 2(b) show SEI image of Au bump, the cross section of micro-bump of the test element group (TEG) respectively. TEG size was 10mm-square and the thickness was 50μm. The bump size was 12μm-square and 1844 bumps were located peripherally.

The hardness of the micro-bumps was measured by Nano-Indentation. The conventional methods such as Vickers test can not measure the hardness of micro-bumps, because of the limitation and size on depth of the indentation. Therefore, Nano-Indentation test was used to measure the hardness on the most surface of micro-bumps by minute force [2]. The hardness was calculated in a following equation (1), where H is the hardness, P_{max} is the peak indentation load, h_{max} is the peak depth, η is the area function and k is the shape coefficient (=24.56: Berkovich indentation), respectively.

$$H = P_{max} / \eta k h_{max}^2 \qquad (1)$$

The hardness was measured by the triangular pyramid indenter with the apex angles of 115°C at the inedent force 3mN.

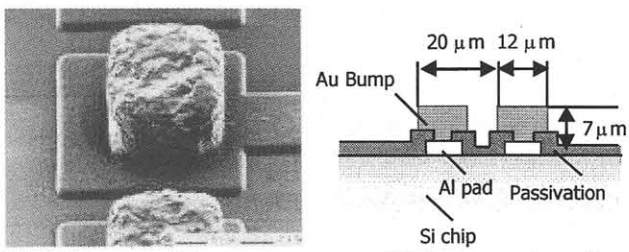
Before the measurement of the hardness, the TEG chips were annealed at 320°C for 15, 30, and 60minutes.

Then, UFB process was performed at 150°C after cleaning of the bump surface with argon sputtering. Figure 3(a) shows the bonding procedure and Figure 3(b) shows the UFB profile.

TEG was bonded to Si interposer that surface was covered with sputtered Au film at 200nm in thickness. The interposer size was 18mm-square and the thickness was 500μm.

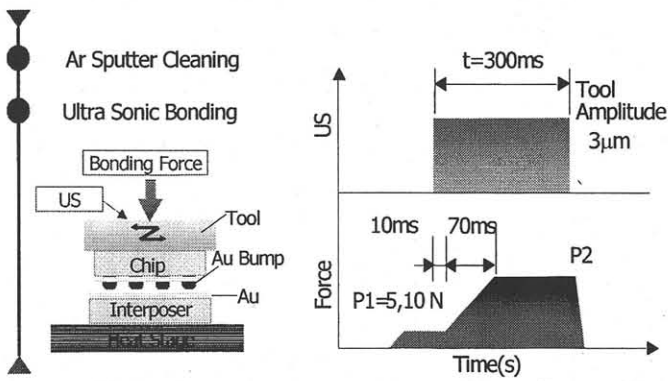
After the bonding, the tensile strength was measured and the fracture mode was investigated to certain the bondability.

In addition, the damage of the chips were inspected at the appearance.



(a) SEI image of Au bumps (b) Cross section of micro-bumps

Fig. 2 Bump structure



(a) Bonding procedure (b) Bonding profile

Fig. 3 UFB Bonding Profile

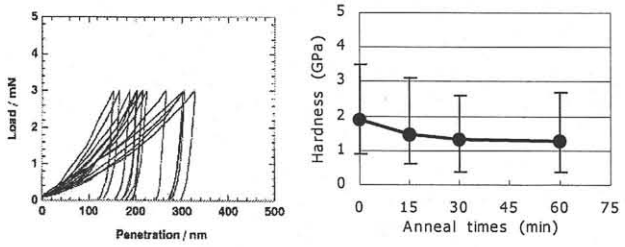
3. Results and Discussion

Hardness of Micro-bump

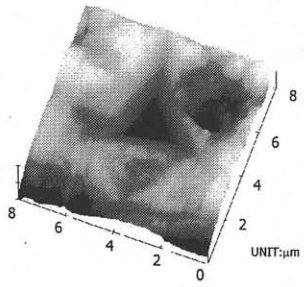
Figure 4 shows the results of the measurement of the hardness and the micro indentation. Figure 4(a), 4(b), and 4(c)

show a sample of P-h curves, the hardness result, the indentation and the surface roughness measured by AFM, respectively. As the anneal times was extended, the hardness decreased and was became stable after 30min. Therefore the condition of the anneal was selected as 30min at 320°C.

However, the deviation of measurement was relatively large. Therefore, it needs further consideration of the optimized measurement.



(a) A sample of P-h curves (b) Result of the hardness of Nano-Indentation



RMS (Rq)	129.53nm
Mean roughness (Ra)	101.31nm
Max height (Rmax)	554.69nm
Box X dimension	2.802μm
Box Y dimension	3.131μm

(c) AFM Image of indentation

Fig. 4 Hardness of Au bumps annealed at 320°C

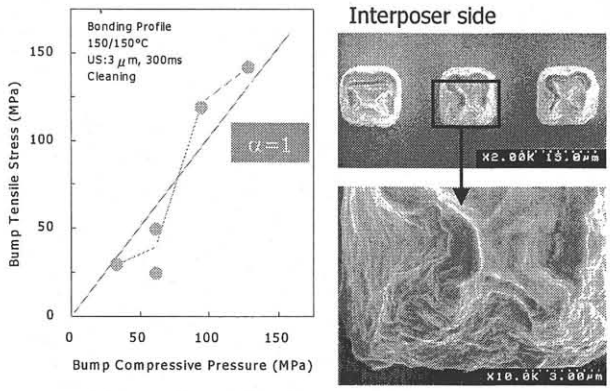
Ultra-sonic Flip-chip Bonding

Figure 5(a) shows the results of the tensile strength measured on the each TEG at the various bonding forces. The bonding strength is indicated as the tensile stress at the each bonding compressive stress for the bump area. The coefficient 'α' is the ratio of the tensile stress against the compressive stress at the flip-chip bonding. In case that 'α' is equal to one, it means that the bonding force is effective to achieve the good bonding strength [3]. The results showed that the coefficient was almost equal to one that suggested sufficient bondability was obtained.

Figure 5(b) shows the fracture interface at the bumps confirmed after the tensile evaluation. The mode was "bulk mode" that indicates the bumps were fractured in the Au, and some portion of the Au bumps were transcribed to the interposer. This suggests that the integrity of the interconnection was accomplished.

Then, Figure 6 shows a photograph of the chip damage. Although no crack was found at the back surface of the Si device, the damage (the black marks) were observed. It is considered that they were generated by the friction between the chip and the bonding tool. If the bonding tool tries to oscillate the chip after the chip is joined to the interposer, the damage will occur to the periphery of the TEG.

Therefore, it is necessary to evaluate the lower bonding profile to optimize the bonding condition.



(a) Tensile evaluation (b) Fracture mode

Fig. 5 UFB Bondability

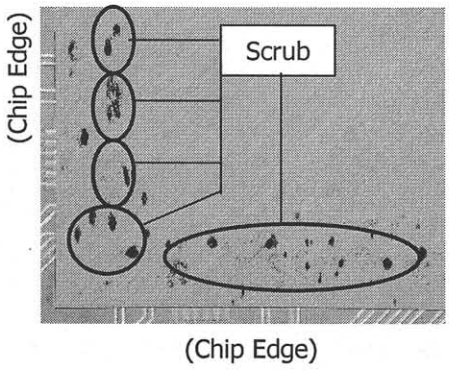


Fig. 6 The damage of TEG after UFB

4. Conclusion

The hardness of micro bump was optimized to realize the low stress bonding. Nano-Indentation test enabled the measurement of micro bump properties, although further consideration to stable the measurement is needed.

Moreover, the ultra-sonic flip-chip bonding was found out to have good possibility as the bonding process. The basic condition to interconnect micro-bumps was realized at the bonding temperature 150°C without chip crack. It needs further consideration of the low force profile, evaluation of the electrical test and reliability.

Acknowledgments

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