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**GIDL Currents in MOSFETs with High-k Dielectric**

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1. Introduction

The thickness of gate oxide cannot be scaled down below 1 nm due to large direct tunneling current [1]. To obtain smaller equivalent oxide thickness, high-k gate dielectric can be adopted for the gate dielectric instead of oxide [2][3]. But the use of high-k dielectric in the conventional device structure can cause severe GIDL current, which induces large consumption of stand-by power in the circuits and loss of charges in the memory cell.

In this paper, GIDL characteristics are compared for different device structures having high-k dielectric as gate dielectric and/or spacer. Guideline to reduce the GIDL current is given in terms of the gate dielectric and spacer structures.

2. Device Structures

In Fig. 1, shown are five different MOSFET device structures used for the analysis of GIDL characteristics. 'Type A' structure has high-k gate dielectric and oxide spacers. In type B, the high-k gate dielectric is extended to the bottom of the spacers. In type C, both of the gate dielectric and the spacer consist of high-k material.

Types D and E have high-k dielectric spacers and SiO2 gate oxides. Type D has the SiO2 gate oxide only under the gate electrode. Physical lengths of the gate and the spacer are 100 nm and 40 nm, respectively.

![Fig. 1. Five different structures with high-k dielectric.](image)

3. Results and Discussions

To see the GIDL current characteristics of each device, extensive 2-D device simulation was performed with conventional physical models. Equivalent oxide thickness (EOT) of the gate dielectric was fixed to be 2 nm. In Fig. 2, GIDL currents with different relative dielectric constants ($\varepsilon_r$) at $V_{GS}=-1$ V and $V_{DS}=1.5$ V are shown. Leakage currents increases rapidly as $\varepsilon_r$ increases for types A and D, slightly decreases for type B and C, and is almost kept constant for type E.

![Fig. 2. GIDL characteristics with different structures and $\varepsilon_r$'s at $V_{GS}=-1$ V and $V_{DS}=1.5$ V.](image)

For types A and D, two materials with different $\varepsilon_r$'s, namely, oxide ($\varepsilon_r=3.9$) and high-k dielectric ($\varepsilon_r>3.9$), meet at the surface of the LDD region. Then the vertical E-field of the region in the high-k dielectric side is greatly enhanced, by which large GIDL current is generated. On the other hand, slight reduction of the leakage current with the increase of $\varepsilon_r$ for types B and C can be explained with the easy penetration of the E-field laterally through the high-k dielectric.

Vertical E-field contours at the surface of the channel and the LDD regions of types A and B are shown in Fig. 3(a) at fixed $\varepsilon_r$ of 40. Abrupt increase of the E-field is shown for type A. In Fig. 3(b), the same contours are shown for type B with $\varepsilon_r$'s of 3.9 and 40. In type B, device with $\varepsilon_r=3.9$ shows higher E-field peak than the device with $\varepsilon_r=40$, which is due to lateral spreading of E-field through high-k gate dielectric.

A layer of SiO2 buffer oxide under the gate dielectric can be a good candidate for the reduction of GIDL current. Fig. 4 shows the GIDL currents with different $\varepsilon_r$'s for types A, B, and C at $V_{GS}=-1$ V and $V_{DS}=1.5$ V. The thickness of the buffer oxide is 6 A and the EOT of the gate dielectric is kept to be 2 nm. GIDL for type A was reduced significantly since the E-field at the surface of the LDD region is diminished due to the buffer oxide. We think it is imperative to adopt the buffer oxide since it relieves not only the GIDL but also material problem between high-k gate dielectric and channel. From the results, the device with type B is a reasonable structure for the suppression of GIDL current although the overlap capacitance can be increased.

To see the effect of the implantation dose of the LDD region on GIDL, LDD implantation dose was changed from

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The GIDL currents are shown in Fig. 5. The gate dielectric thickness (εr=25) was assumed since it is the most commonly used high-k material. The implantation dose of LDD region increases. The GIDL current also increases significantly since large lateral straggle of implanted ions results in increased overlap region between the gate and LDD region.

Until now, leakage characteristics have been compared at the fixed EOT of 2 nm. In this case, the physical thickness of high-κ gate dielectric increases as εr increases. Then the DIBL becomes severe as shown in Fig. 6. It is also worth while to compare the GIDL characteristics based on constant DIBL.

Fig. 7 shows GIDL characteristics with constant DIBL of 60 mV/V for types A, B, and C. The EOT becomes thinner with the increase of εr, and GIDL current increases. Again, type B shows the best GIDL characteristics.

4. Conclusions

GIDL characteristics have been studied for different device structures having high-κ dielectric as spacer and/or gate dielectric. The structures were compared in terms of dielectric constant, EOT and DIBL. Also E-field contours which are responsible for the GIDL were shown. It is concluded that device structure having a gate dielectric stack of high-κ gate dielectric/buffer SiO2 and SiO2 spacer is reasonable for the suppression of GIDL. As the EOT becomes smaller by using high-κ, the GIDL becomes severe.

Acknowledgments

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References