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## A New Circuit Simulation Model of Ferroelectric Capacitors

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### 1. Introduction

A simulation model of ferroelectric capacitors is essential for accurate circuit simulation of ferroelectric memories. Several models have been proposed[1]-[5]. They reproduce either time and voltage dependence of polarization switching, or hysteresis loops under arbitrary applied voltage. But it has been difficult to describe both behaviors by a single model because of their complicated characteristics. In this report, we propose a model which reproduces both of the behaviors under any condition using simple SPICE elements. Results of circuit simulation using this model are also shown.

### 2. Parallel Element Model

The model consists of multiple sets of a capacitor and a resistor connected in parallel as shown in Fig. 1. This represents the distribution of coercive voltage and switching polarization mentioned in ref.[2]-[5]. Each element is supposed to show an independent response to a voltage change, which is obtained by measuring the responses at various combination of voltage steps and solving the matrix. The details of the measurement sequences are described in ref.[6]. From the measurement, it reveals that the switching behavior of each capacitor element is reproduced by a capacitor which has a hysteresis loop of parallelogram and a resistor of which the conductance is proportional to the power of voltage.

This result is implemented to a SPICE model by modifying the model presented by Sheikholeslami et al.[3] A capacitor element is expressed by a set of voltage controlled current source (VCCS) and a voltage controlled capacitor (VCC). The current is zero when the voltage on VCCS is below  $V_D$ , which is equivalent to the coercive voltage. When the voltage is larger than  $V_D$ , the current controls the voltage dependence of switching speed. The square function of VCC gives the value of switching charge, where  $V_C$  gives the center voltage of the loop and  $\Delta V_C$  determines the width of lateral of the parallelogram.

### 3. Simulation Results

Simulation results on a  $\text{SrBi}_2\text{Ta}_2\text{O}_9$  capacitor are shown in comparison with the measurement data. Figure 3 shows the pulse response at various applied voltage.

The capacitor was polarized at -3 V, then switched at each voltage. The rise time of the pulse was set to 10 ns to simulate the actual measurement condition. The roughness of the curves is due to discontinuous distribution of coercive voltages used in the model. Figure 4(a) shows the frequency dependence of the hysteresis loops. The loop width was larger for higher frequencies, because the polarization could not switch fast at low voltages. Figure 4(b) shows the comparison of minor loops under asymmetric applied voltage. The full loop was measured at 5 kHz. Calculated result showed a good agreement with the measured data.

### 4. Circuit Simulation

Memory operation was simulated using this model. The circuit used for the simulation is shown in Fig. 5. In this operation, the plate line was kept at 0 V, and data on ferroelectric capacitors were read out by applying a pulse at A shown in the figure to charge bitlines through the resistors. The size of ferroelectric capacitors, bitline capacitance and the resistance were  $1 \mu\text{m}^2$ , 100 fF and 10 k $\Omega$ , respectively. When the bitlines are charged, the capacitor C0 which stored data '0' switches and show larger capacitance than C1 ('1'), then it should cause delay in rising of BL0 level.

Simulation result is shown in Fig. 6 (a). The rise time of the pulse was 5 ns. When the operation voltage was 5V, voltage difference between the bitlines appeared after the voltage became larger than 3 V. This means if the sense amplifier is activated before this point, the data may be misread. In case the operation voltage was 3V, only a small voltage difference appeared. To verify the influence of switching speed, simulation was done with setting the switching speed  $10^3$  times faster so that it was faster than RC time constant of the circuit (Fig. 6 (b)). The voltage difference appeared from the beginning in this case. Therefore, ferroelectric materials which can switch fast at low voltage are necessary for this type of operation.

### 5. Summary

A new ferroelectric capacitor model for SPICE simulation has been developed. The model reproduced the time and voltage dependence of polarization under any condition in good agreement with the measured data.

Circuit simulation using this model showed the influence of the switching speed on actual device operation.

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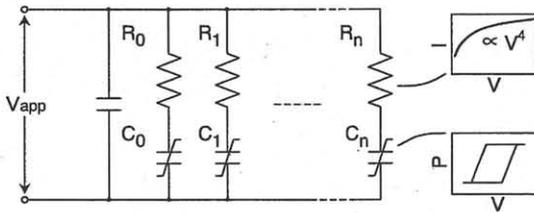


Fig. 1 The parallel element model of a ferroelectric capacitor. Each element has different coercive voltages and switching polarization.

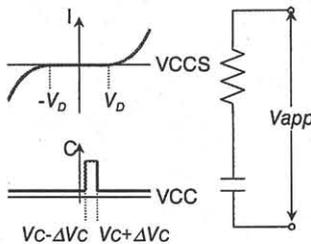


Fig. 2 SPICE model of a capacitor element.

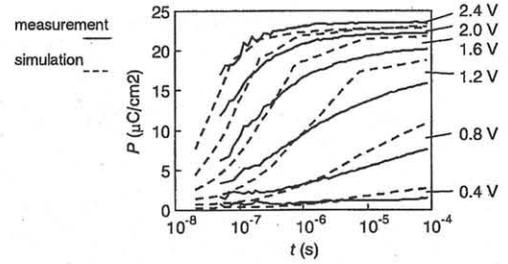


Fig. 3 Measured and simulated pulse response of SrBi<sub>2</sub>Ta<sub>2</sub>O<sub>9</sub> capacitor.

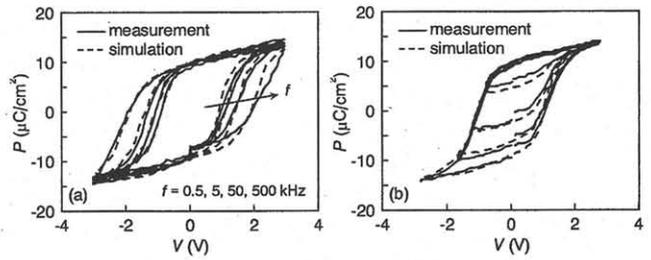


Fig. 4 (a) Frequency dependence of hysteresis loops. (b) Minor loops measured at 5 kHz.

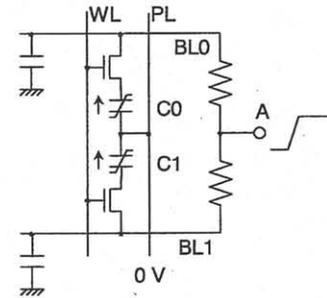


Fig. 5 The circuit of memory cells used for the simulation. Plate line was kept at 0 V.

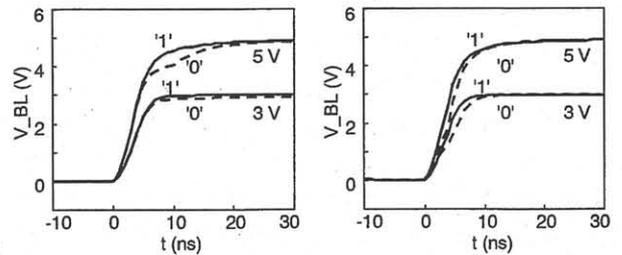


Fig. 6 Simulation result of bitline voltage change (a) using the model from measured switching data, (b) using the model with the switching speed much faster than the time constant of the circuit.