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Non-Volatile Doubly Stacked Si Dot Memory with Si Nano-Crystalline Layer

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1. INTRODUCTION

To improve the charge retention in Si dot memory [1], we have shown that the Si self-aligned doubly stacked dot memory [2] attains better charge retention, because the energy barrier in the lower dot (ΔE) due to Coulomb blockade and quantum confinement suppresses charge leak between upper dot and channel effectively in low VG. Fig.1 shows retention improvement factor of doubly stacked Si dot memory compared to the usual single dot memory [2]. This is the tunnel probability ratio between single and double tunnel junctions in low VG, and depends on ($\Delta E/T$) exponentially. Upper x-axis shows a measure of corresponding lower dot diameter. According to this theoretical prediction, lower dot size scaling is essential to realize a low-voltage non-volatile memory.

In this work, we propose a doubly stacked Si dot memory with Si nano-crystalline layer, which contains 3nm size lower Si dots densely (Fig.2). Since the dense lower dots are formed by annealing thin a-Si layer, they can be scaled down simply by making the initial a-Si thinner. We demonstrate that the Si doubly stacked dot memory with nano-crystalline layer can retain sufficiently wide memory window for 10^8 sec. The results clearly show that the lower dot scaling has a great impact on charge retention as our prediction, and Si doubly stacked dot memory is very promising.

2. EXPERIMENT

A cross-sectional TEM view of the doubly stacked Si dot structures is shown in Fig.3, and crystal stripes can be found in the 3nm Si layer. The typical lower crystalline dot size is 3nm. The 3nm thick Si layer, which was initially a-Si layer formed by CVD, is mostly poly-crystallized by anneal processes in device fabrication, because 3nm thick a-Si is crystallized in higher temperature than 900C [3]. The point is that the lower dot size can be controlled by the initial a-Si layer thickness and the anneal process. We also fabricated the usual single Si dot memory with single 3nm thick tunnel oxide without lower dot layer, and nano-crystalline layer memory without upper dots.

3. RESULS AND DISCUSSION

3-1. Memory effects due to upper dots

Fig.4 shows ID-VG characteristics of the doubly stacked dot memory, the usual single dot memory and the nano-layer memory. We note that the memory effects in the doubly stacked dot memory is due to charging to the upper dots, since the memory effect of the nano-layer memory without upper dots is very small. We also find that the memory window of the double dot memory is larger than the usual single dot memory.

3-2. 10^5 times improvement by 3nm lower dot

To study the retention improvement quantitatively, we examine charge retention in inversion region. In the double dot memory (Fig.5), the charge retention is about 10^5 times longer than the single dot memory (Fig,6), since ΔVth at 10^5sec corresponds to ΔVth at 1sec of single dot memory.

This 10^5 times improvement corresponds to the energy barrier ΔE=0.35eV (Fig.1), and this will be possible value for 3nm lower Si dot. So, the improvement is considered to be due to high ΔE in 3nm lower dot. To confirm our ΔE theory, we show lower dot size and temperature dependence.

3-3. Lower dot size dependence

Fig.7 shows the cross-sectional TEM view of a doubly stacked dot memory with 5nm size lower dots. For the larger lower dot memory, the retention is 100 times longer than the single dot memory (Fig.8). 100 corresponds to ΔE=0.15 eV (Fig.1), and this is almost consistent with 5nm lower dot size. This is a proof of our ΔE effects.

3-4. Temperature dependence

For ΔE = 0.35 eV, the retention improvement at 400K is 1/20 of that at 300K (Fig.1). Fig.9 shows the retention characteristics at 400K. The retention time at 400K is indeed about 1/20 of that at 300K, while no such reduction is found in single dot memory. This is another proof of ΔE theory.

3-5. Charge retention

We examine the charge retention of the double dot memory in sub-threshold region (Fig.10). Excellent charge retention is achieved in the double dot memory. According to our ΔE theory, the double dot memory will retain 4 orders in ID magnitude at 10^8 sec, because the memory window at 10^3 sec of the single dot memory corresponds to that at 10^8 sec of the double dot memory. The above results show a great impact of lower dot size scaling on charge retention.

4. CONCLUSION

The great impact of lower dot size scaling on charge retention has been shown. The Si nano-crystalline layer doubly stacked dot memory shows 10^5 times longer retention time, and will retain 4 orders in ID after 10^8 sec. Further improvement is very easy, since we are allowed to make upper dot density higher and lower Si dot size smaller. It is concluded that Si doubly stacked dot memory is a strong candidate for future low-power non-volatile memory.

References

[1] S.Tiwari et al.,: IEDM Tech. Dig. (IEEE 1995) p. 521
[2] R.Ohba et al.,: IEDM Tech. Dig. (IEEE 2000) p.313
[3] P.Persans et al., J. of Non-crystalline States **102** (1988) 130

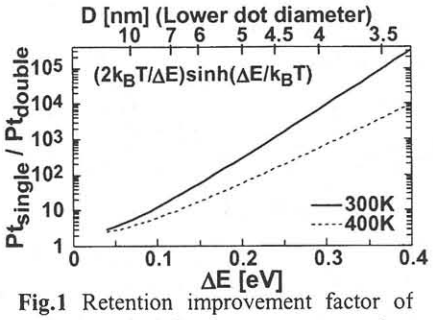

Fig.1 Retention improvement factor of doubly stacked dot memory compared to usual single dot memory.

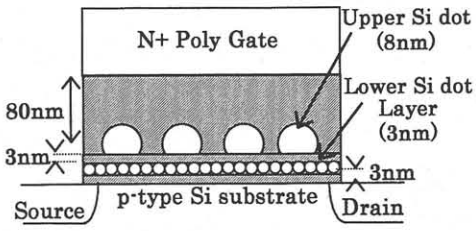

Fig.2 Schematic diagram of Si nano-crystalline layer doubly stacked dot memory.

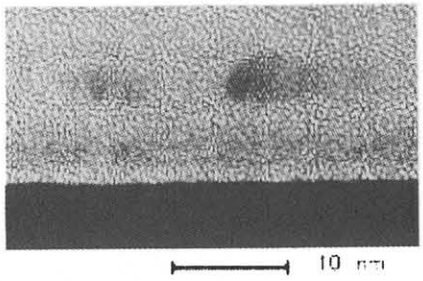

Fig.3 Cross-sectional TEM view of Si nano-crystalline layer double dot memory.

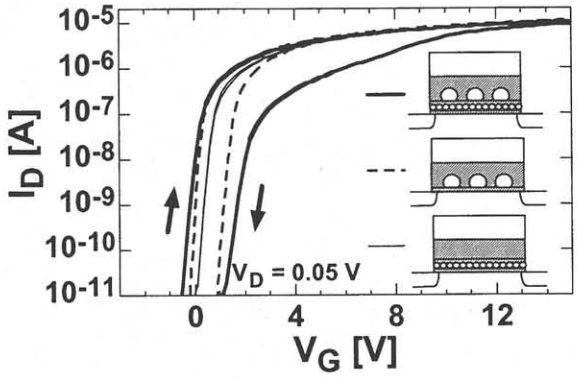

Fig.4 Id-Vg characteristics of the Si double dot memory, usual single dot memory, and nano-layer memory.

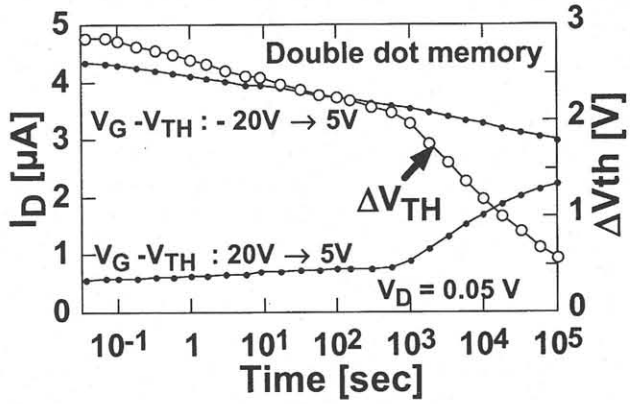

Fig.5 Retention characteristics for double dot memory at VG-VTH= 5V after write/erase at 20 / - 20 V for 1 sec.

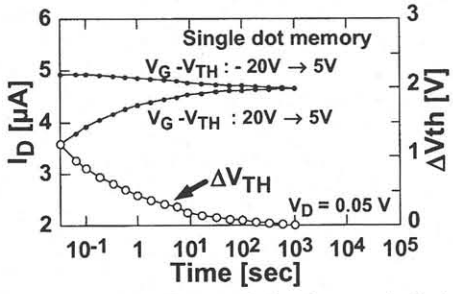

Fig.6 Retention characteristics for usual single dot memory in linear region.

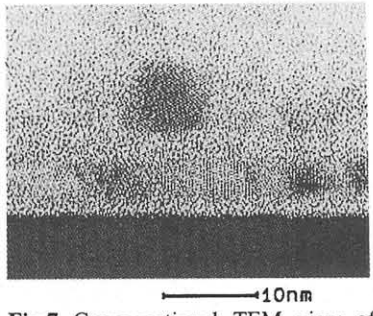

Fig.7 Cross-sectional TEM view of the doubly stacked dot memory with 5nm lower dot layer.

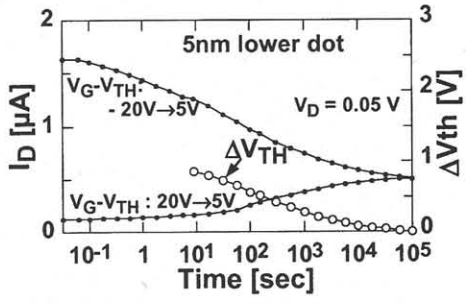

Fig.8 Retention characteristics in linear region for the double dot memory with 5nm lower dots.

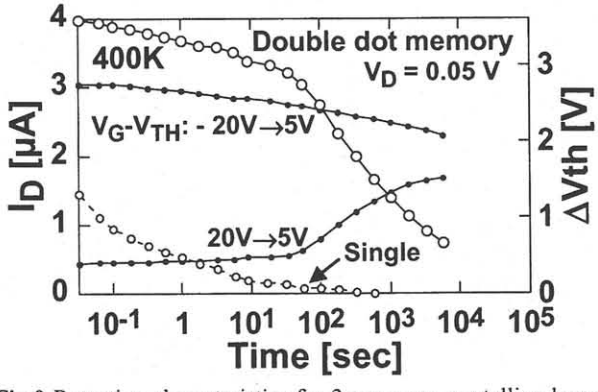

Fig.9 Retention characteristics for 3 nm nano-crystalline layer double dot memory, in linear region at 400K. Δ Vth for single dot memory at 400K is also shown for comparison.

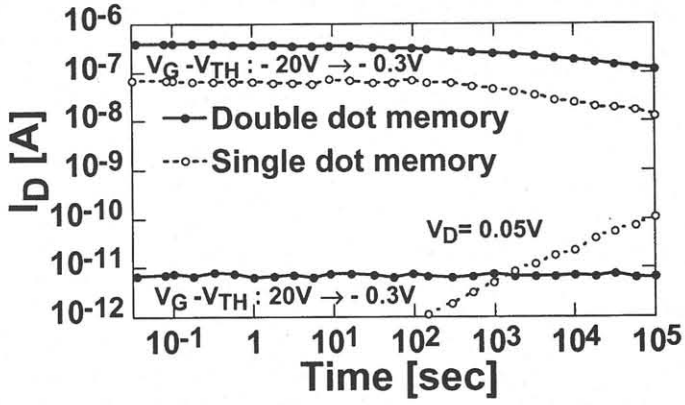

Fig.10 Retention characteristics at VG-VTH= - 0.3V after write /erase at 20 / - 20 V.