# LF-1-3 Field-Dependent Mobility of Highly Oriented Pentacene (C<sub>22</sub>H<sub>14</sub>) Thin Film FETs

T. Komoda, Y. Endo, K. Kyuno and A. Toriumi

Department of Materials Science, Graduate School of Engineering, The University of Tokyo 7-3-1, Hongo, Tokyo 113-8656, Japan Phone:+81-3-5841-7161 Fax:+81-3-5841-7161 E-mail:komoda@adam.t.u-tokyo.ac.jp

# 1. Introduction

Much progress has been made in recent years in the field of organic thin-film transistors(TFTs)<sup>[1]-[4]</sup>. Organic TFTs have many advantages in terms of low cost processing, mechanical flexibility, or versatile material selectivity. These properties make organic devices very attractive for enabling electron devices in the next generation.

Pentacene( $C_{22}H_{14}$ ) is a promising material, because it has been reported that its TFT has a relatively high mobility<sup>[3]</sup>, and can operate as an ambipolar device<sup>[2]</sup>. However, the mobility is still low for a practical use. To achieve higher TFT performance, it is strongly required to make clear of the carrier transport mechanism in the FET channel in detail.

This paper reports the fabrication of pentacene TFT, the modification of pentacene film, and the analysis of carrier transport in the FET channel. In particular, the carrier mobility is discussed as functions of both lateral and perpendicular electric fields in the FET structure.

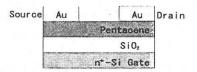
#### 2. Device Fabrication

The pentacene thin film layer was evaporated in a vacuum on 33nm-thick SiO<sub>2</sub> thermally grown on the surface of a heavily doped n<sup>+</sup> silicon wafer. The vacuum evaporation was typically performed under the base pressure of about 10<sup>-6</sup> Pa, the deposition rate of 0.05nm/s, and the substrate temperature of 25°C. To modify or to hopefully improve the pentacene film quality, a thermal treatment at 50°C for an hour in a vacuum was employed for a part of the samples. The device reported in this paper has approximately 50nm-thick pentacene film, and 30nm Au electrodes for source/drain contacts were thermally evaporated on the top of the film. The gate length and width were both 500µm. Fig.1 is a schematic cross section of the pentacene TFT. The heavily doped silicon substrate acts as the gate electrode. X-ray diffraction and atomic force microscope (AFM) were used for characterizing structural qualities of the film.

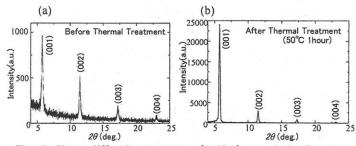
### 3. Results and Discussion

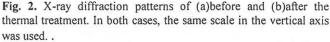
Fig.2(a) and (b) show the x-ray diffraction patterns of pentacene films before and after the thermal treatment. In both cases, no other phase rather than the thin film phase<sup>[5][6]</sup> was observed. Furthermore, note that the 50  $^{\circ}$ C, 1hour thermal treatment significantly improves the molecular ordering (more than 20 times in the intensity ratio).

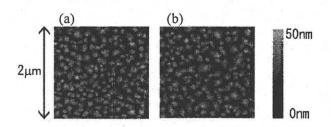
Fig.3(a) and (b) show AFM images of the film surfaces before and after the thermal treatment. In Fig. 3(a), the grain size is about  $0.3\mu$ m, while in Fig. 3(b), some of the grains grows larger. It looks like that some adjacent grains combined with each other. It is also found that the RMS



**Fig.1.** Schematic diagram of pentacene TFT device. The  $n^+$  silicon was used for gate electrode, while the thermally grown SiO<sub>2</sub> was used for gate insulator. Au was deposited as source and drain electrodes on the pentacene layer.







**Fig.3.** AFM images of (a)before and (b)after the thermal treatment. Scanned area is  $2\mu m \times 2\mu m$ . It is observed that the grain size becomes slightly larger by the thermal treatment

value of the pentacene top surface is reduced from 8.1nm to 6.7nm in the 10x10  $\mu m^2$ 

The Id-Vg and Id-Vd characteristics of the pentacene FET are shown in Fig.4 and Fig.5. Both results clearly demonstrate that the device fabricated in this work operates very well as a conventional p-FET with a long channel. The subthreshold coefficients of devices before and after the thermal treatment were approximately the same or it might be slightly degraded, though the structural property was significantly improved. Note that the highest mobility value we obtained is about 0.2cm<sup>2</sup>/Vsec, which is in the world's top class value so far reported <sup>[1]-[4]</sup>.

To further investigate the carrier transport in the FET channel, the filed dependence of the mobility was

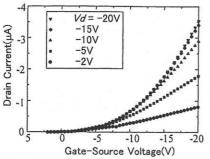


Fig.4. Id-Vg characteristics of the pentacene TFT before the thermal treatment.

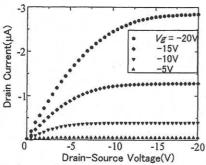


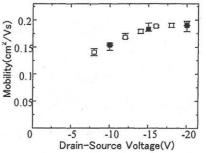
Fig.5. Id-Vd characteristics of the pentacene TFT before the thermal treatment.

investigated. The mobility was extracted from Id-Vg characteristics as a function of the drain-source voltage in the saturation region (the field effect mobility), and also from Id-Vd characteristics as a function of the gate-source voltage in the linear region (the effective mobility). Fig.6 shows the drain-source voltage dependence of the field effect mobility. Solid and open points represent before and after the thermal treatment, respectively. Furthermore the gate bias dependence of the effective mobility in the linear region is shown in Fig.7. We have noticed the time dependent degradation or recovery of I-V characteristics during measurements, which apparently caused some inconsistency between the results in Fig. 6 and 7. But, in this paper we focus on the electric field dependence of the channel mobility. As shown in Fig. 6 and 7, the mobility increases with both lateral and perpendicular fields. The results can be reasonably understood from the viewpoints of filed-induced barrier lowering in the channel the (Pool-Frenkel type barrier lowering in the lateral direction)<sup>[4]</sup>, and the screening effect of free carriers (including the effective barrier lowering at the grain boundaries), respectively.

On the other hand, when it is considered that the structural properties were significantly improved by the thermal treatment as discussed before, the mobility results suggest that the pentacene FET mobility is dominantly determined by the interface qualities at the grain boundary and/or the pentacene/SiO<sub>2</sub> rather than macroscopic molecular ordering in the high mobility regime.

#### 4. Conclusions

We have investigated the pentacene FET and obtained



**Fig.6.** Drain-Source voltage dependence of the filed effect mobility. Solid( $\blacksquare$ ) and open( $\square$ ) squares correspond to before and after the thermal treatment, respectively. All points were extracted from saturation region fitting in *Id-Vg* characteristics at *Vg*=-10V.

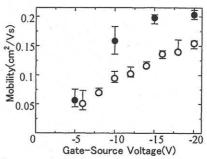


Fig.7. Gate-Source voltage dependence of the effective mobility. Solid( $\bigcirc$ ) and open( $\bigcirc$ ) squares correspond to before and after the thermal treatment, respectively. All points were extracted from the slope of *Id-Vd* characteristics at *Vd*=0.

 $\mu$ =0.2cm<sup>2</sup>/Vs for the p-channel FET. Furthermore, the thermal treatment effects on the film properties and the field dependent mobility were discussed. The results indicate that the thermal treatment improves significantly the molecular ordering of the film, but that it affects little on the carrier mobility. Moreover, the field dependence of the mobility implies that the interface qualities at the grain boundary and/or the pentacene /SiO<sub>2</sub> limit the FET performance in high quality films. Finally, it is addressed that there is another engineering point of improving the interface in addition to the macroscopic molecular ordering, in order to achieve high performance organic FETs.

#### Acknowledgments

This work was partly supported by SCAT and Toshiba R&D Center.

# References

- C. D. Dimitrakopoulos, D. J. Mascaro, *IBM J. Res. & Dev.*, 45, p.11(2001).
- [2] J. H. Schön, S. Berg, Ch. Kloc, B. Batlogg, Science, 287, p.1022(2000).
- [3] H. Klauk, D. J. Gundlach, J. A. Nichols, T. N. Jackson, *IEEE T-ED*, 46, p.1258(1999).
- [4] G. Horowitz, Adv. Mater., 10, No. 5, p.365(1998).
- [5] T. Minakata, H. Imai, M. Ozaki, J. Appl. Phys., 72, p.5220(1992).
- [6] C. D. Dimitrakopoulos, A. R. Brown, A. Pomp, J. Appl. Phys., 80, p.2501(1996).