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A New CMOS Passive Mixer with High Linearity

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1. Introduction

Recently, as the feature size of CMOS transistors is reduced, CMOS technologies are good candidate for RF-IC applications[1]. To achieve the goal of reducing the power consumption, the passive mixer is preferred in recent low power transceivers. It has extremely low power consumption and high linearity. Several passive ring mixers using CMOS technology are realized in [1-3]. However their core consists of only NMOS switches, which results in limited linearity. This paper presents a new CMOS passive mixer, which has additional PMOS switches to improve the linearity characteristics.

2. Circuit Design

The conventional NMOS passive mixer[2] has the following problem: To turn the NMOS switch on, the gate voltage of the NMOS switch should be greater than the source voltage by the threshold voltage. Therefore, the output IF signal is severely compressed when incoming RF signal is large compared to the LO signal. This output limiting problem significantly degrades the linearity of the mixer. The technique that solves this problem is to add PMOS switches in parallel with NMOS switches. Finally, the proposed CMOS mixer schematic is shown in Fig. 1. Fig. 2 shows the simulated AC transfer characteristics of NMOS and CMOS switches. The gate biases of NMOS and PMOS are 2.5 V and –2.5 V, respectively. For the case of NMOS switch, as the input amplitude increases, there is output compression because of the V_T drop problem. While, as shown in Fig. 2, the CMOS switch is free of the V_T drop problem due to the PMOS operation, which can improve the 1-dB compression point (P1dB) performance. Fig. 3 shows the full circuit diagram of the proposed CMOS mixer. Because the incoming RF signal is unbalanced but the proposed mixer is double balanced structure, the on-chip balun, XF1 is used to convert the incoming unbalanced signal to the balanced signal. A on-chip square symmetric transformer was used as a passive balun at the RF input terminals for low power consumption[4]. The probe buffer (MN5-MN8) at the output, included for measurement purpose, presents a high impedance load to the mixer. The drain of the buffer is left open for measurement convenience.

3. Measurement Results

The proposed CMOS mixer is fabricated in a 0.25μm 5-metal CMOS technology. The microphotograph is shown in Fig. 4. The chip area of the fabricated mixer is 0.14mm^2. Fig. 5 shows the measurement configuration of the test chip. The output pads of the test chip are connected directly to the PCB(printed circuits board) by the wire bonding. For the measurement purpose, the LO signal is converted into differential signal using off-chip balun. In the measurement, the RF frequency was 2.401 GHz and the LO frequency was 2.4 GHz. The supply voltage is 2.5 V and the power consumption except output buffer is about 0.4 mW, which almost consumes the bias circuit. All possible loss components in the measurement, such as cable, connector, and impedance mismatch losses, were de-embedded from raw measurement data. Also de-embedding of the output buffer was performed. The measured input-referred 1-dB compression point at the LO voltage of 0.495 V_{PP} is –0.4 dBm (Fig. 6). In Fig. 6, the power conversion gain is about –14.5 dB. Fig. 7 shows the LO voltage dependence of the voltage conversion gain. As the LO voltage increases, voltage conversion gain increases. At the LO voltage of 0.495 V_{PP}, the voltage conversion gain is about –0.17 dB. Fig. 8 shows the results of two-tone third-order intercept point (IP3) measurement with tones at 2.40095 GHz and 2.40105 GHz. The applied LO voltage is 0.495 V_{PP}. The measured input-referred IP3 is about 12.5dBm. The LO to RF isolation is one of important characteristics, because the LO signal can radiate through the antenna and affect the neighboring receivers. The measured LO port to RF port isolation was 41.2 dB, which is satisfied typical demand of 30 dB. LO feed-through is decreased by using CMOS switch[5]. Table I summaries the measured performance of the proposed CMOS mixer and compares with the other reported works. The linearity characteristics of the proposed mixer are much superior to the other reported works.

4. Conclusions

A new CMOS passive ring mixer using CMOS switches instead of NMOS switches has been presented. The proposed mixer shows superior linearity especially on P1dB characteristics by solving the output-limiting problem due to the V_T drop of the NMOS switches. The feasibility of the proposed mixer was demonstrated by implementing in 0.25μm 5-metal CMOS technology.

Acknowledgments

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References

[1] T. Lee et al., Proceedings of the IEEE, 1560, (2000).

[2] A. R. Shahani et al., IEEE JSSC, **32**, 2061, (1997).

[3] Penny Gould et al., 2000 IEEE MTT-S Int., **1**, (2000).

[4] J. R. Long, IEEE JSSC, **35**, no. 9, 1368, (2000)

[5] Sandstrom, T, Circuits and Systems, 2000. 42nd Midwest Symposium on, **2**, 834, (2000).

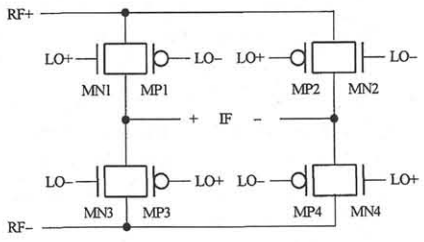

Fig. 1 Proposed CMOS passive mixer schematic.

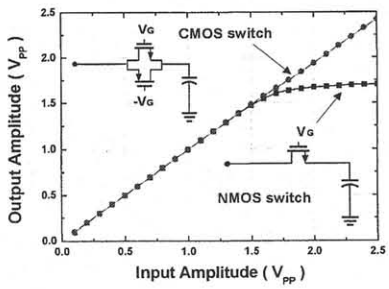

Fig. 2 Simulated AC transfer characteristics of NMOS switch and CMOS switch at the gate bias of 2.5 V.

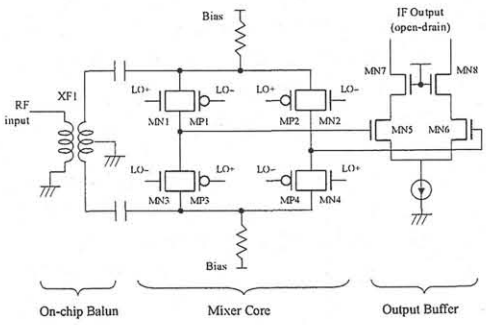

Fig. 3 Full circuit diagram of the proposed CMOS mixer.

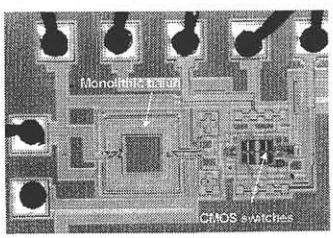

Fig. 4 Microphotograph of the proposed CMOS mixer.

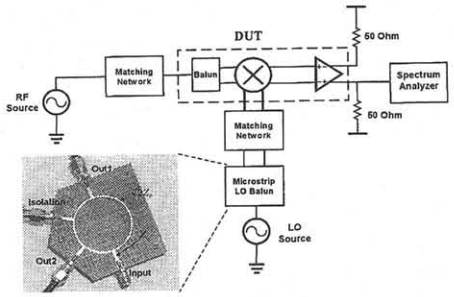

Fig. 5 Measurement set-up.

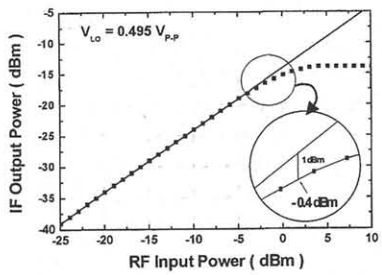

Fig. 6 Measured input 1dB compression point at the LO voltage of 0.495 V_{PP}.

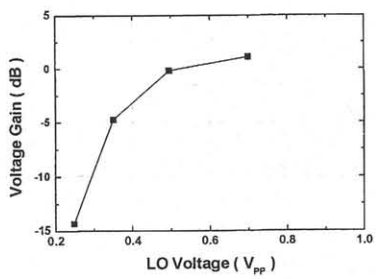

Fig. 7 The LO voltage dependence of the measured voltage conversion gain.

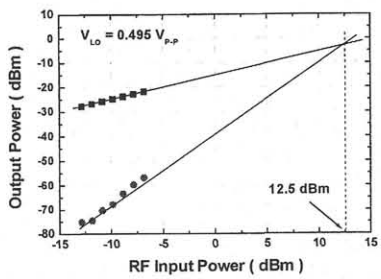

Fig. 8 Measured input IP3 characteristic at the LO voltage of 0.495 V_{PP}.

Table I Performance summary and comparison

	This works	[4]	[5]
Architecture	Transformer+CMOS switch	NMOS switch	NMOS switch
Operating frequency	2.4 GHz	1.4 GHz	1.8 GHz
LO voltage/power	0.495 V_{PP}	0.6 V_{PP}	4 dBm
Power conversion gain	-14.5 dB	-	-6.9 dB
Voltage conversion gain	-0.17 dB	-3.6 dB	-
Input-referred P1dB	-0.4 dBm	-5 dBm	2.9 dBm
Input-referred IP3	12.5 dBm	10 dBm	11.1 dBm
LO to RF isolation	41.2 dB	-	-
Power dissipation	0.4 mW	-	-
Technology	0.25μm CMOS	0.35μm CMOS	0.25μm BiCMOS
Chip area	0.14 mm^2	0.84 mm^2	1.8 mm^2