Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, Tokyo, 2001, pp. 422–423

P-1-12

Novel Methods to Incorporate Deuterium in the MOS Structures and Isotope Effects on Soft Breakdown and Interface States

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1. Introduction

It is believed that the hydrogen passivates the Si/SiO_2 interface trap density and improves the device performance [1]. However, the device performance still degrade due to hydrogen desorption from Si/SiO_2 interface by hot electrons [2]. Lyding reported that hot carrier induced degradation is improved by replacing hydrogen with deuterium during the sintering process [3]. While the integration of deuterium incorporation into the CMOS manufacturing process is still a concerned issue. We report a new approach to enhance deuterium incorporation at Si/SiO_2 interface by a process sequence of high vacuum pre-bake, deuterium pre-bake, and deuterium post-oxidation anneal.

2. Novel Deuterium Incorporation Methods

The Si wafers are cleaned by a HF dip before the oxidation, and Si surface is passivated by hydrogen. To incorporate deuterium in the rapid thermal oxide, the wafer is baked at 1000°C and 500 mbar for 2 min in deuterium, and then oxide is grown, followed by a 900 °C nitrogen anneal for 10 min. The SIMS profiles (Fig.1) of this deuterium pre-bake process show a deuterium concentration of $2x10^{19}$ cm^{-3} in the oxide. To further increase the deuterium incorporation, a post-oxidation deuterium anneal is added before the nitrogen anneal in the previous process. This yields a deuterium concentration of $2x10^{20}$ cm^{-3} (Fig. 2). The hydrogen passivated surface after the HF dip prevents the deuterium incorporation to some degree. The passivated hydrogen layer can be desorbed in the high vacuum (HV, < 10^{-6} torr) bake before the deuterium bake. With the HV bake, the deuterium incorporation in the oxide can reach as high as $9x10^{20}$ cm^{-3} (Fig. 3). The grown oxide thickness by the deuterium is 10-20% smaller, as compared to the hydrogen process. For all three processes, the deuterium atoms not only distribute at Si/SiO_2 interface but also in the entire SiO_2 layers, very similar to deuterium pyrogenic oxide [4]. The incorporation of deuterium both at interface and bulk oxide plays an important role to suppress the electron trap creation. Note that the pyrogenic oxidation [4] yields a much lower deuterium concentration of $1x10^{19}$ cm^{-3}, as compared to our process.

3. Isotope Effects on Oxide Soft Breakdown and Dit

Under constant current stress biased at negative gate voltage, the NMOS (Al gate electrode, t_{ox} less than 3 nm) tunneling diodes do NOT reveal an apparent isotope effect (Fig.4&5) at low current density (<0.2A/cm^2). At high current density (~3A/cm^2), the deuterium-treated devices show improved soft breakdown and SILC characteristics (Fig.6&7). Heavily doped substrates (~0.03 Ω-cm) are used to avoid the series resistance effect. Note that no isotope effect on SILC was observed in deuterium post-metal anneal process [5], which has deuterium distribution only at Si/SiO_2 interface. A resonance relaxation model is proposed to explain these effects (Fig.8) [6]. Due to the resonance with Si lattice, the vibrational excited state of Si-D bond has smaller decay time, as compared to Si-H bond. The low current stress (long impact interval) can not reveal the isotope effect if the impact interval is longer than both decay times. The isotope effect can only be observed when the impact interval is between the decay times of Si-D and Si-H bonds. Under this situation, the Si-D bond excited states will relax to lower energy states, since the decay time is shorter than the impact interval, while Si-H excited states can be further excited and eventually jump over the bonding barrier, since the subsequent electron impacts the excited S-H bonds before the decay event. Due to the tunneling current of MOS diodes with ultrathin oxide, it is difficult to extract D_{it} using the conventional C-V method. The band-edge light emission [7,8] is, therefore, used to monitor the D_{it}. The increase of D_{it} increases the tunneling current through the D_{it}, and degrades the light emission intensity at constant current drive. Fig.9&10 show the significant degradation of light intensity of H_2-treated devices as well as SILC (the insets), as compared to D_2-treated devices. This indicates the increase of D_{it} in the H_2-treated device. From the time evolution measurement (Fig.11), the D_{it} increases rapidly at initial 1000 sec stress, and saturates up to 10000 sec stress. For D_2-treated devices, the light intensity slightly increases in the initial stress due to the self-annealing, but no degradation is observed for light intensity and SILC. To confirm this observation, we perform the C-V measurement on MOS diodes with thick oxide (5 nm), the extracted D_{it} increases by ~7x in H_2-treated devices after stress, while no apparent increase of D_{it} is observed in D_2-treated devices (Fig.12).

4. Conclusions

These novel methods can have deuterium distribution not only at interface but also in the bulk oxide and can obtain high deuterium concentration. The isotope effects on SILC, soft breakdown, and D_{it} are observed. Highly reliable gate oxide can be obtained, as compared to the conventional deuterium post-metal anneal process.

Acknowledgments

This work is supported by NSC, R.O.C.

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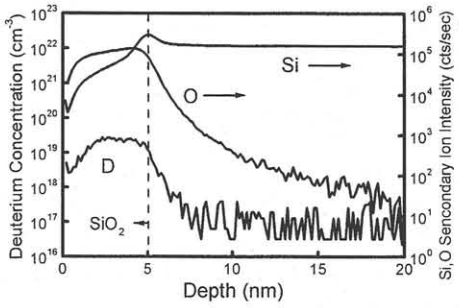

Fig. 1 SIMS profiles of the rapid thermal oxide with deuterium pre-bake.

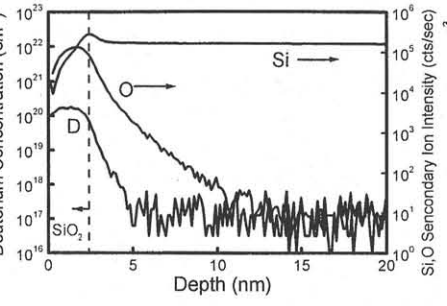

Fig. 2 SIMS profiles of the rapid thermal oxide with deuterium pre-bake and the post-oxidation deuterium anneal.

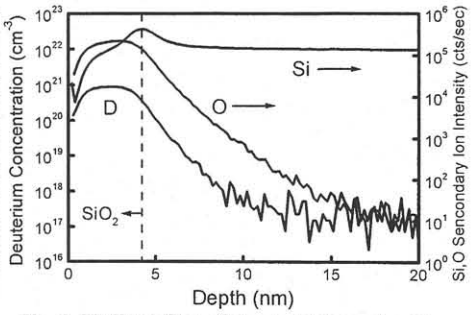

Fig. 3 SIMS profiles of the rapid thermal oxide with HV pre-bake, deuterium pre-bake and the post-oxidation deuterium anneal.

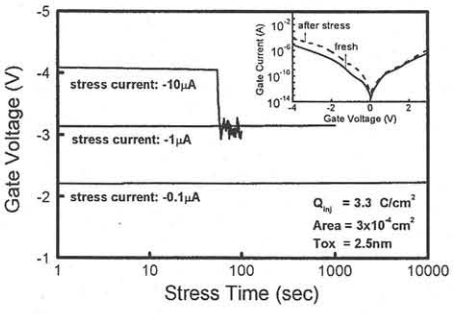

Fig. 4 The gate voltage vs stress time plot of H_2-treated NMOS diodes under different low current density injection. The inset is the current-voltage characteristics of device before and after -10 μA CCS.

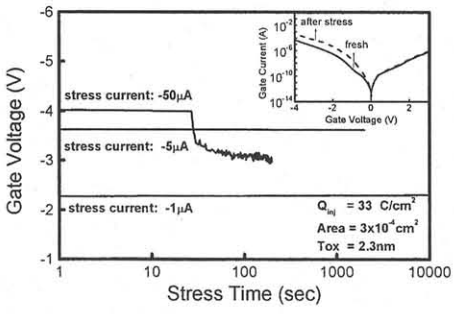

Fig. 5 The gate voltage vs stress time plot of D_2-treated NMOS diodes under different low current density injection. No improvement is observed in D_2-treated devices.

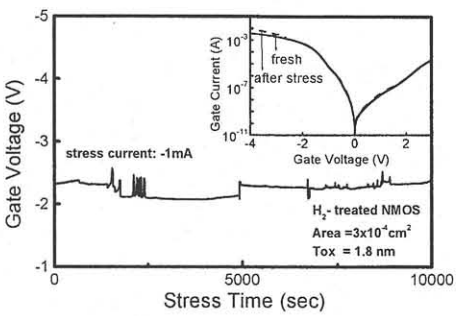

Fig. 6 High current stress of H_2-treated NMOS diodes. Soft breakdown occurs after ~1000 sec stress. The inset is the current-voltage characteristics of device before and after stress.

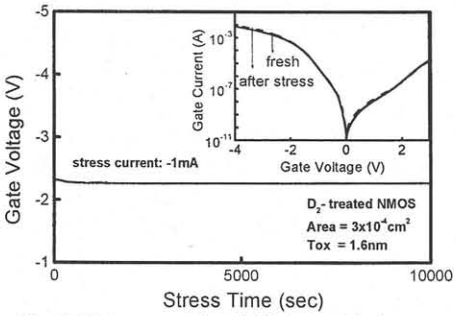

Fig. 7 High current (low initial gate bias) stress of D_2-treated NMOS diodes. No apparent fluctuation in gate voltage is observed. Improvement is observed in D_2-treated devices at such high current stress.

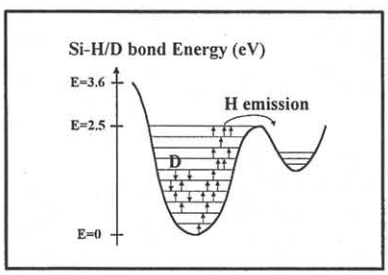

Fig. 8 The schematic diagram of the speculative mechanism of Si-H/D bonds desorption. Isotope effect can be observed on the D_2 devices due to the relaxation back to low energy states. The hydrogen is up-pumping to the transport mobile states via multiple vibrational excitation.

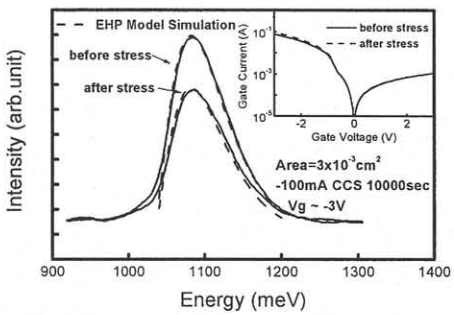

Fig. 9 The electroluminescence of the H_2-treated NMOS diodes before and after stress. The stress condition is –100 mA for 10000 sec. The inset is the I-V before and after stress. This degradation of intensity indicates the increase of Dit after stress.

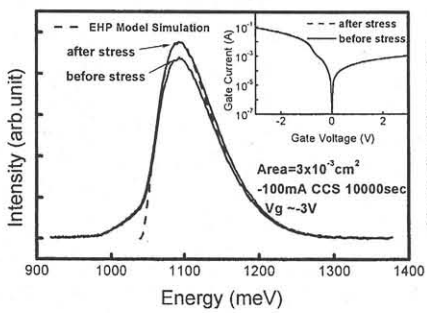

Fig. 10 The electroluminescence of the D_2-treated NMOS diodes before and after stress. The inset is the current-voltage characteristics of device before and after stress.

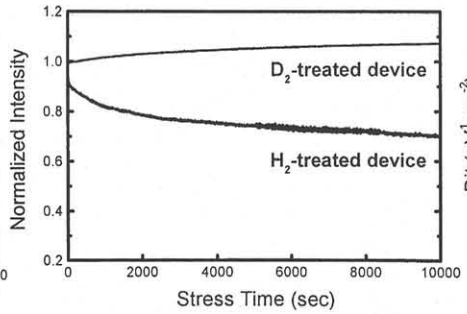

Fig. 11 Time evolution of the emission intensity at peak for both H_2-treated and D_2-treated NMOS diodes. The initial increase of light intensity of D_2-treated sample is probably due to self-annealing.

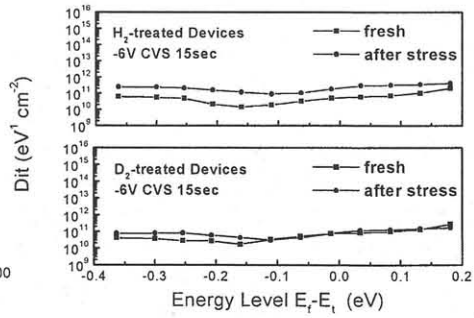

Fig. 12 The interface states density vs energy level of H_2 devices (up) and D_2 devices (down) before and after stress. Approximate 7x increase of D_{it} after stress in H_2 devices. No apparent increase of D_{it} in D_2 devices.