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Optimization of Low Power Shallow Trench Isolation BiCMOS Technology for Mixed Analog/Digital Application Systems

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1.Introduction

Low power BiCMOS technology is useful for mixed analog/digital applications, such as mobile telecommunications systems. In these applications, both high-frequency operation and low noise characteristics are required around 2 or 5 GHz for analog part by BJT, and low power digital operation such as PLL by CMOS is also important. We demonstrated a bipolar technology using deep and shallow trench isolations which offers a low parasitic structure [1]. And then we reported a BiCMOS technology which is combined with 0.3μm CMOS and passive components [2]. Passive components, such as MIM capacitor, are indispensable for analog applications. However, the integration of high performance BiCMOS with MIM capacitor has the serious problem of large leakage current in the off-stage of CMOS which is also isolated by shallow trench isolation, as a results, low power consumption is not achieved successfully .

In this paper, we describe the process optimization of low stress isolation technology for low power BiCMOS ,which includes high frequency epi base bipolar, 0.3 μm CMOS, and passive components.

2.DEVICE FABRICATION

The process steps of this BiCMOS ware well described in [2]. A high performance epi-base double-polysilicon NPN transistor , a 0.3 μm CMOS, two types of polysilicon resistors of which sheet resistances are 400Ω per square and 2KΩ per square, a high precision capacitor and an inductor are implemented on the same silicon wafer. Figure 1 shows the process steps of this BiCMOS, which consist of four parts.

Bipolar Frontend

Shallow trench defines the active areas of both BJT and CMOS. The depth of shallow trench is about 0.7μm. Deep trench is used only for BJT, and its depth is about 5.5μm.

CMOS Devices Formation

Because the formation of gate electrodes should be fine patterning, it is suitable to form the CMOS devices on the planarized field before BJT process.

Implantation of PMOS S/D is also used for doping of L-PNP collector and emitter.

NPN Device Formation

Base poly electrode is also used as polysilicon resistor layer. P+ implant for base poly electrode is also used for doping of low resister. Combination of 900C 10min annealing by furnace and 985C 20sec annealing by RTA is carried out for activation of emitter and CMOS S/D diffused layers. After this activation, base and emitter poly electrodes are silicided by titanium in order to reduce the parasitic resistances.

Capacitor

MIM capacitor is formed with SiN of 50nm between the emitter polysilicon electrode, which is titanium silicided, and the first metal layer.

Metal interconnection

An inductor was formed with the second metal layer.

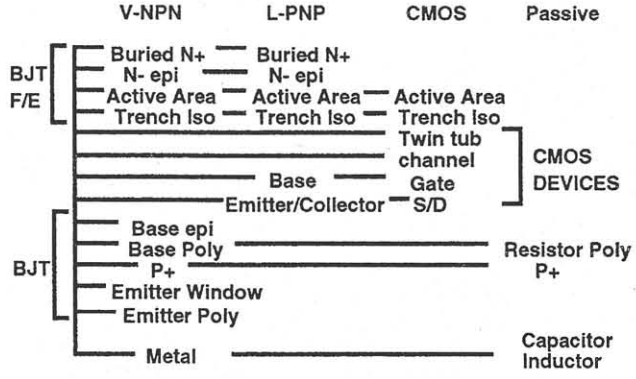

Figure 1 Process of this BiCMOS

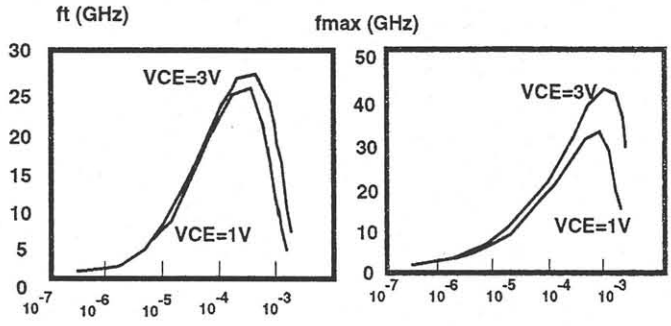

Figure 2 f_T and f_{max} vs. collector current

3.DEVICE CHARACTERISTICS AND DISCUSSION

The cut-off frequency (fT) and the maximum oscillation frequency (fmax) have been obtained by the S-parameter measurement. An fT of 27GHz at 3V Vce and an fmax of 43GHz at 3V Vce are obtained, as shown in Figure 2(a) and in Figure 2(b) respectively.

Figure 3 shows the process dependence of the NMOS subthreshold characteristics with a gate width of 10μm and gate length of 0.45μm. In the case of pure CMOS without BJT and MIM capacitor process, ID@VG=0V is less than 1E-11A, however in the case of BiCMOS, ID@VG=0V is larger than 1E-11A. This means large power consumption of CMOS logic circuits in stand-by stage. This problem must be prevented in order to realize low power operation. Several papers report that boron diffusion or segregation are enhanced by mechanical stress [3], [4] .

In taking account of this phenomena, we assume that mechanical stress, which is caused by STI as shown in Figure 4 (a), makes diffusion and segregation coefficient enhanced and boron concentration around STI edge are reduced under the thermal process steps of bipolar and capacitor formations, as shown in Figure 4 (b), as a result, parasitic low Vth transistors are formed around STI edge. In order to prevent this problem, it is effective that thermal budget should be reduced.

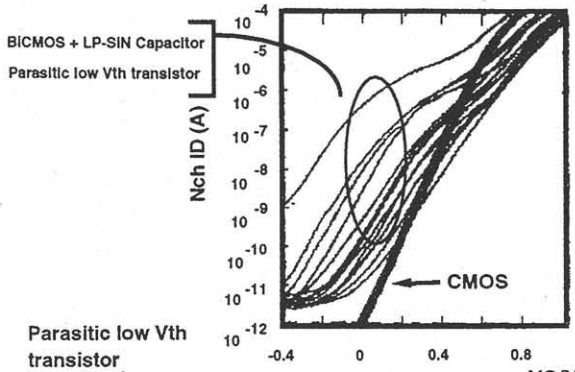

Figure 3 Process dependence of NMOS ID-VG characteristics

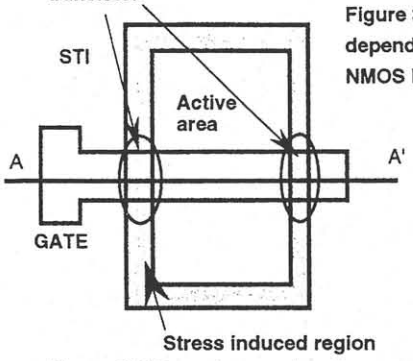

Figure 4(a) Over view explanation. Stress is induced at STI edge by STI structure

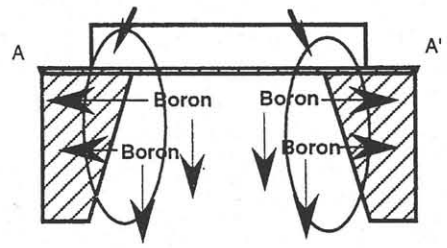

Figure 4(b) Cross sectional explanation. Boron diffusion is enhanced by the stress, as a results, the channel boron concentration is reduced.

The leakage current level is slightly improved with low temperature capacitor dielectric deposition process from 780C to 380C, however, it is not sufficient compared with pure CMOS case.

Although this result suggests the requirement of additional reduction of thermal budget, it is difficult to reduce the bipolar thermal budget without sacrificing the bipolar transistor performance. This means that the mechanical stress itself should be reduced.

Generally, in order to reduce the mechanical stress around STI edge, it is effective to optimize the STI structure.

Figure 5 shows the dependence of leakage current @ VG=0V on STI angle obtained from NMOS subthreshold characteristics. As the STI angle decreases around 60 degree, leakage current is reduced significantly. Figure 6 shows the improved NMOS subthreshold characteristics with plasma enhanced low temperature (380C) deposited SiN, and the STI angle of around 60 degree .

On the other hand, PMOS subthreshold characteristics has no problem even in BiCMOS case with LP-CVD SiN Capacitor and the STI angle over 60 degree. We assume that comes from the different dependence of diffusion mechanism on stress between As ,Phos and Boron.

In table 1 , the typical device parameters of NPN are summarized. The typical characteristics of 0.3μm CMOS (Vds=Vgs=3.3V) are summarized in Table 2. The typical output characteristics of NMOS and PMOS are shown in Figure 7.

4.CONCLUSION

We have optimized the low power BiCMOS technology featuring NPN of 42GHz fmax , 0.3 μm CMOS, and passive components. The key point of this BiCMOS integration is low stress process. With the STI angle optimization and the plasma enhanced low temperature (380C) deposited SiN, high performance BiCMOS with MIM capacitor without large leakage current was realized. These features contribute to the creation of high performance BiCMOS LSIs for various mixed analog / digital applications.

5.ACKNOWLEDGMENT

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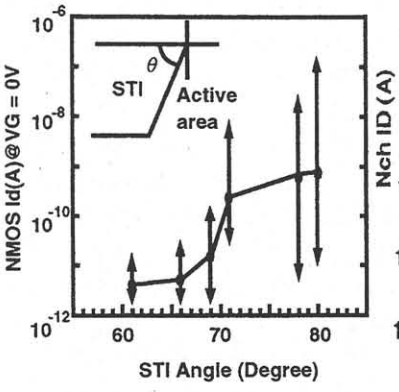

Figure 5 STI angle dependence of NMOS ID@VG=0 in case of BiCMOS with Plasma SiN Capacitor

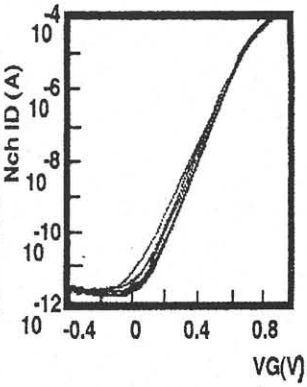

Figure 6 Finally improved NMOS ID-VG characteristics of full optional BiCMOS

Table.1 BJT device parameters

	BJT
Emitter size (μm2)	0.3 X 1.0
hFE	70
Cje (fF)	5.2
Cjc (fF)	2.6
Cjs (fF)	12.3
Re (Ω)	60
Rb (Ω)	615
BVebo (V)	3.4
BVcbo (V)	19
BVceo (V)	7.7
peak fT (GHz)	27
peak fmax (GHz)	42
Va (V)	76

Table.2 CMOS device parameters

	NMOS	PMOS
Leff	0.3	0.3
Tox (nm)	9	9
Vth (V)	0.58	-0.61
Idr (μA/μm)	492	-196

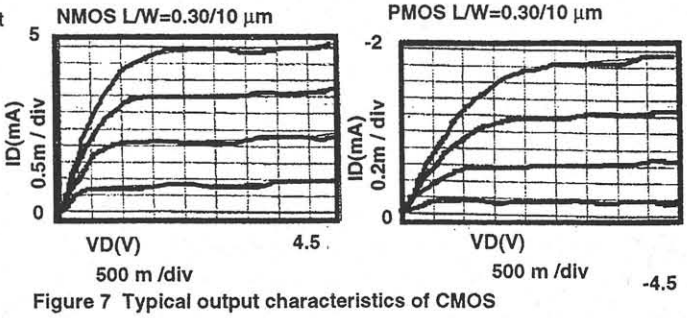

Figure 7 Typical output characteristics of CMOS

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