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Single Electron Memory with a Defined Poly-Si Dot Based on Conventional VLSI Technolgy

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1. Introduction

As the cell size of memory devices is reduced rapidly, the number of electrons that determine the memory cell states is decreased and the thermal energy is comparable to the charging energy in the memory node. Single electron memories are good candidates to overcome these physical limits[1]. In general, there are two types in single electron memory nodes. One is single quantum dot[2,3] and the other is nanocrystal array[4,5]. Nanocrystal memories show large threshold voltage shifts and good retention characteristics relatively. But, since the whole memory cell is not scaled down, there are fluctuation problems due to dot size difference. Single dot memories have very small memory node size that is suitable for ultimate scale down, but it is difficult to define a small quantum wire and dot. Mainly, e-beam lithography is used to define quantum wires and dots. However, long time and high cost are required in patterning (low throughput). Besides, as scaling down proceeds, undesirable phenomena such as proximity effect arise.

In this research, we have implemented a novel patterning method based on conventional VLSI technology named as sidewall masking technique. Sidewall masking technique has a good uniformity and controllability in size of defined patterns as well as high throughput. Applying this patterning method, single electron memories with self-aligned poly-Si dots on narrow channels were fabricated.

2. Fabrication of single quantum dot

Figure 1 shows the process sequence for fabrication of single quantum dot on a narrow channel. At first, tunnel oxide is grown on Si thin film and poly-Si is deposited. Next, a buffer layer is deposited on the poly-Si. Then, Si_3N_4 is deposited and patterned by photolithography and poly-Si is deposited. Subsequently, poly-Si sidewall is formed by etching. After the remaining Si_3N_4 is wet-etched, the oxide layer is patterned using the sidewall as a mask. The poly-Si, tunnel oxide and Si layer are all anisotropically etched to define a narrow wire. Si_3N_4 is deposited again and patterned perpendicularly to cross over the above-mentioned wire. Then, the previous sequence of steps is repeated except that anisotropic etching is stopped at tunnel oxide layer. Figure 2 shows the cross section of 30nm-wide Si quantum wire defined by sidewall masking technique. To inspect the uniformity of line width, we measured the electrical conductance of wires. Figure 3 shows the distribution of normalized electrical conductance of 50μm long wires defined by the sidewall masking technique and e-beam lithography. Measured wires have 60nm width in sidewall masking technique and 80, 130nm width in e-beam lithography. The standard deviation of conductance is 12% of average value in the sidewall masking technique. But in e-beam lithography, the standard deviation is each 78%, 30% of average value. Especially, 80nm wires patterned e-beam have very small conductance because there are very slender parts in the middle of wires due to irregular patterning. Figure 4 shows a poly-Si quantum dot defined by the sidewall masking technique. Its planar size is about 30nm×35nm before reduction by thermal oxidation.

3. Characteristics of the fabricated devices

Fabricated devices have thin 3nm tunnel oxide and 30nm control oxide. Figure 5 shows the hysteresis characteristics of the fabricated device. The control gate bias was swept up from 0V to 8V and swept down in backward. The threshold voltage shift is about 0.24V. The devices have good I_d-V_g characteristics: subthreshold swing is 76mV/dec and I_{on}/I_{off} ratio is 10^6 even though they have very narrow channels (30nm). Figure 6 shows the threshold voltage as a function of the programming voltage at 300K and 5K. The devices show quantized threshold voltage shift due to coulomb blockade effect at room temperature. In fact, different devices were measured at each temperature, but they have similar ΔV_{th} and ΔV_P values of 50mV and 300mV, where ΔV_{th} is threshold voltage shift amplitude and ΔV_p is the interval of programming voltages between the quantum jump. From the measured values, the capacitance between the quantum dot and the control gate is calculated to be about 0.53aF[1]. It is estimated from the capacitance value that the effective size of the quantum dot is about 20nm×25nm. Considering that the quantum dot in Fig. 4 is further reduced by an additional thermal oxidation, this is consistent with the geometry of the defined quantum dot. Figure 7 shows the retention time of fabricated devices. Though the tunnel oxide is thin in direct tunneling region, devices show good retention characteristics almost until 5×10^3 s.

Summary

Single electron memories were fabricated using conventional VLSI technology named as sidewall masking technique. The wires defined by the sidewall masking technique have a good uniformity in line width. Fabricated devices show quantized threshold voltage shift at room temperature and have good output characteristics and retention time.

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Reference

[1] K. Yano, et al., *IEEE Trans. Electron Devices* vol.42, p1628, 1994.
[2] S. Tiwari, et al., *Appl. Phys. Lett.*, vol.68, p1377, 1996.
[3] I. Kim, et al., *IEEE Electron Devices Lett.*, vol.20, p630, 1999.
[4] L. Guo, et al., *Appl. Phys. Lett.* vol.70, p850, 1997.
[5] A. Nakajima, et al., *Appl. Phys. Lett.* vol.70, p1742, 1997.

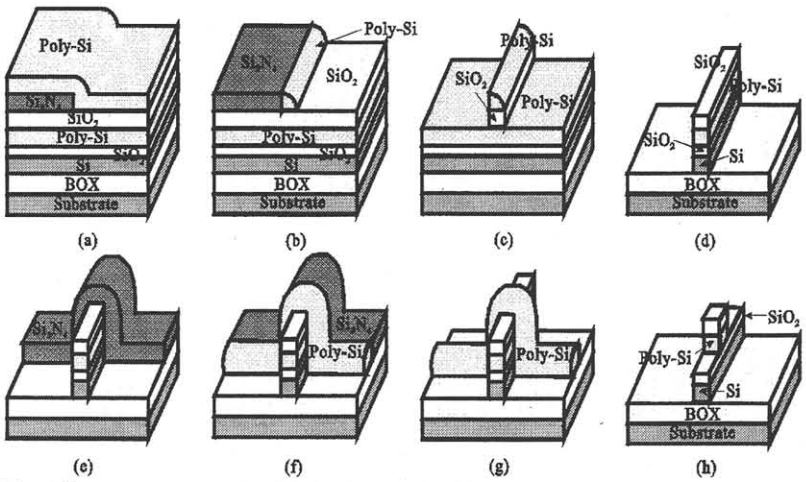

Fig. 1 Process sequence for fabrication of single quantum dot on SOI wafer.

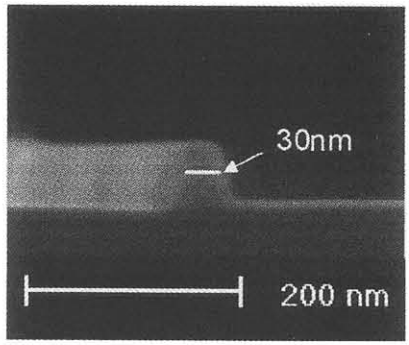

Fig. 2 SEM image of Si quantum wire with 30nm line width.

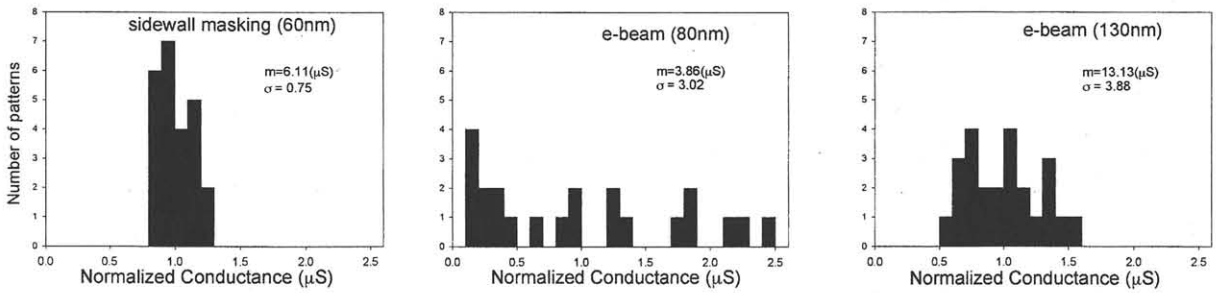

Fig. 3 Normalized electrical conductance of wires defined by sidewall masking technique and e-beam lithography.

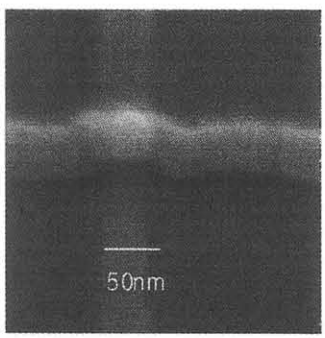

Fig. 4 SEM image of poly-Si quantum dot before thermal oxidation

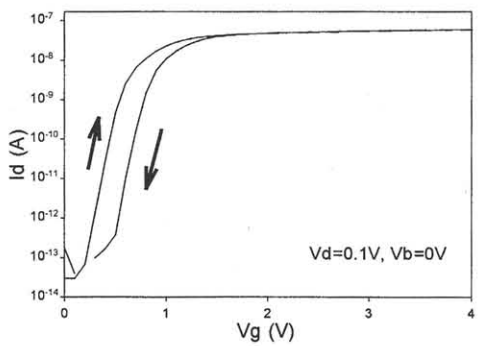

Fig. 5 Hysteresis characteristics of the fabricated devices.

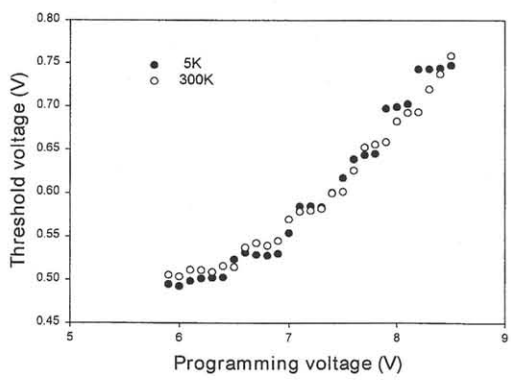

Fig. 6 Program characteristics of the fabricated devices.

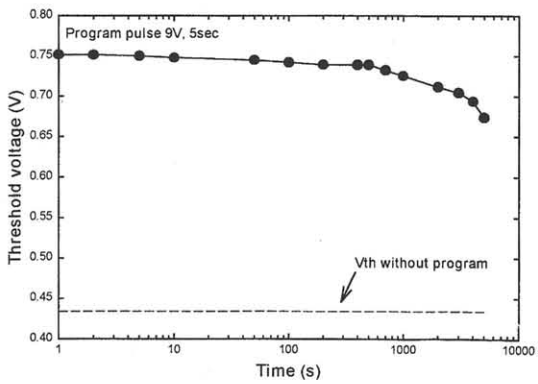

Fig. 7 Retention characteristics of the fabricated devices.