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Optimisation of Tunnel Barriers for nc-Si Single-Electron Transistors

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1. Introduction

We have previously reported the fabrication of nanocrystalline silicon (nc-Si) films which contain crystalline silicon (c-Si) grains < 10 nm in size embedded in an amorphous silicon matrix[1]. These c-Si grains can behave as charging islands in a single-electron transistor (SET). Due to the small grain size, nc-Si films are suitable materials in which we can fabricate SETs operating at high temperature. However, the tunnel barriers formed by the a-Si in the grain boundaries does not constitute a high potential barrier to confine electrons onto the charging islands, especially at room temperature[2]. However SETs oxidized at 1000°C for 15min, have demonstrated the fabrication of SETs in large grained polycrystalline silicon (poly-Si) films[3] to be too resistive. In addition such a high temperature oxidation was found to increase grain size significantly. In this paper we propose a simple thermal process to engineer the tunnel barriers so that they will be high enough for room temperature single-electron charging effects.

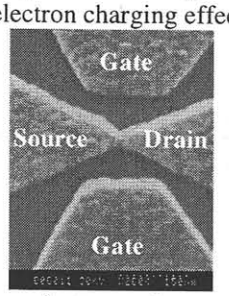

Figure 1 A scanning electron micrograph of a fabricated device. There are two side gates separated from the channel by 120 nm.

2. Material and device fabrication

A 20-nm-thick nc-Si film is grown on a 150 nm thick buried oxide layer thermally grown on a crystalline silicon substrate. A 100 MHz-VHF plasma-enhanced chemical vapor deposition (PECVD) method from a SiF_4, H_2 and SiH_4 gas mixture is used[1].

SETs are fabricated by means of electron beam lithography. The device structure is shown in Fig. 1. The source and drain electrodes meet at a point contact with a width of 20 nm.

3. Tunnel barrier engineering

In the as-deposited nc-Si SET, single-electron effects persist up to 60 K. From the Arrhenius plot of the device, we obtain a maximum activation energy of 40 meV. This corresponds to the maximum barrier height in the as-deposited material[2].

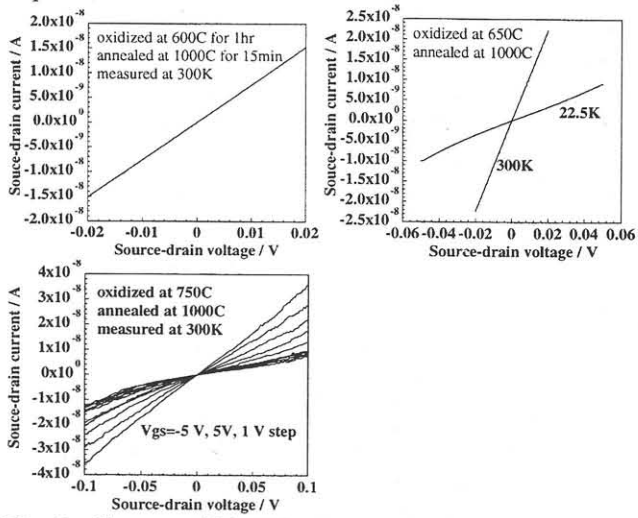

Fig. 2 Change of Ids-Vds characteristics at 25K and 300K by oxidation

We calibrated the effect of oxidation temperature on the electrical characteristics of the nc-Si SETs in improving the tunnel barrier property. We systematically varied the oxidation and annealing temperature Oxidation duration was fixed at 1hr (Fig. 2). After oxidizing at 600 °C and annealing at 1000 °C, the device exhibits Ohmic conduction at 300 K and 20 K. By increasing the oxidation temperature to 650 °C and keeping the same annealing temperature, the resistance of the device increases and it is non-linear at 22.5 K. Finally, oxidizing at 750 °C and annealing at 1000 °C we can obtain non-linearity even at 300 K with observable gating effects.

The Arrhenius plot of the oxidized and annealed device shows that the tunnel barrier height has increased from 40 meV to 170 meV (Fig. 3). Preliminary study using poly-Si films and nanowires indicated that the low oxidation process resulted in selective oxidation of the grain boundaries and the subsequent annealing process converted the oxidized grain boundaries to silicon oxide with high barrier height. The low temperature oxidation process form silicon sub-oxide SiO_x (x<<2) via the oxygen diffusion through the grain boundaries. It was confirmed that the sub-oxides formed at low temperature have low barrier height. Annealing at 1000 °C causes chemical bond restructuring in the sub-oxide resulting in stronger Si–O bonds.

The oxidation and annealing process did not cause significant changes to the grain size of the nc-Si film.

Transmission electron microscope (TEM) micrographs show that the c-Si grains remain approximately the same in size (see Fig.4).

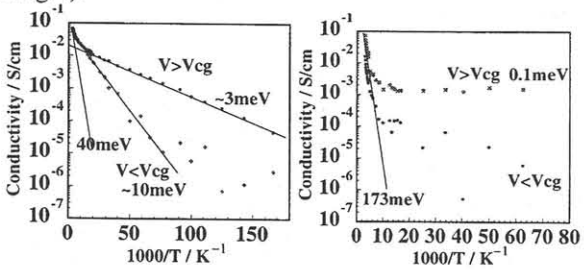

Fig. 3 Arrhenius plot of conductivity for as-deposited (left) and oxidized/annealed (right) devices.

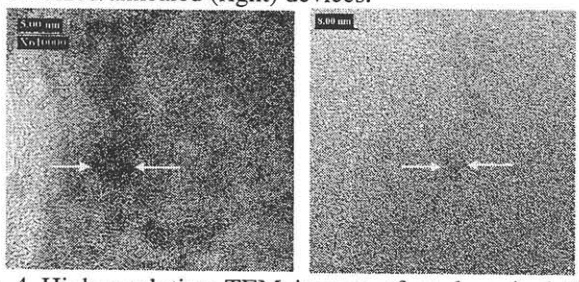

Fig. 4 High-resolution TEM images of as-deposited (left) and oxidized/annealed (right) devices.

4. Electrical results

We observe clear single-electron charging effects in the device and the results measured at 77 K are shown in Fig. 5. From the I_{ds}-V_{ds} characteristics we obtain a Coulomb blockade region of ~ 100 mV and the I_{ds}-V_{gs} plot reveals a current oscillation period of ~ 3V. We measured the temperature dependence of these electrical characteristics and found that the single electron charging effects persists up to 300 K (see Fig. 6). From these results we are able to estimate the charging island to be ~ 7 nm in diameter, similar to the c-Si grain size as observed by TEM.

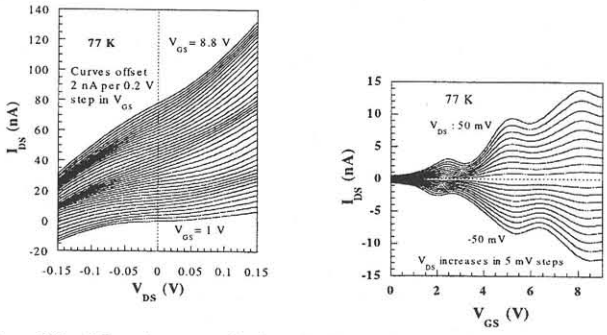

Fig. 5 I_{ds}-V_{ds} characteristics (left) and gate-bias conductance oscillation (right) of the oxidized and annealed device measured at 77K.

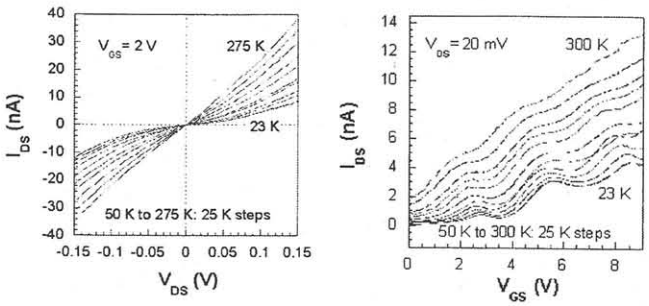

Fig. 6 Temperature dependence of I_{ds}-V_{ds} characteristics (left) and gate-bias conductance oscillation (right).

5. Conclusions

We have investigated the oxidation process to improve the electrical characteristics of nc-Si SETs. It was found that the combination of the low temperature oxidation followed by higher temperature annealing formed good tunnel barrier with ~170 meV in height without changing the charging island size. The SETs exhibited single-electron charging effects up to 300 K. Further optimisation is in process so as to obtain better electron confinement onto the charging island at temperatures >300K.

Acknowledgements

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References

[1] T. Kamiya, K. Nakahata, Y.T. Tan et al., J. Appl. Phys. (June, 2001) in print.

[2]Y.T.Tan, T. Kamiya, Z.A.K. Durrani and H.Ahmed, Appl. Phys. Lett. **75**, 797, (2001).

[3] Y.T.Tan, Z.A.K.Durrani, H.Ahmed, J. Appl. Phys. **89**, 1262 (2001).