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Three Dimensional Size Evaluation of Island in Si Single-Electron Transistor

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1. Introduction

A single-electron transistor (SET) is a candidate for a key device in future LSIs [1-3]. The fabrication method named pattern-dependent oxidation (PADOX) that we have developed is one of the simplest methods for making small SETs as it can form a small SET island together with tunnel barriers at both sides in a self-aligned manner. The theoretical model of Si-SET [4] predicts that the SET island is generated by oxidation-induced stress at the central part of the Si wire and the rest of the wire act as tunnel barriers. In order to confirm this model, it is necessary to evaluate the relationship between the actual Si-wire length and the effective SET-island length.

In this paper, we evaluated the three dimensional size of SET using SEM and AFM, and we determine the effective length of the SET island from the relations between the electrical characteristics and the measured structures.

2. Imaging of the embedded Si structures

To clarify the relation between the island size and electrical characteristics, we observe the structure of the device whose characteristics had already been measured electrically. We remove the gate electrodes which cover the island by wet etching. Since we have developed the imaging technique of the embedded structure using scanning electron microscopy (SEM) with nanometer-order resolution [5], we can observe the main component of the SETs that is a Si nanowire embedded in SiO_2. As shown in Fig. 1, an image of the embedded Si is clearly observed in the secondary electron mode using a 30 kV electron beam. The outline of the embedded Si is represented by dotted lines. The Si-wire width and length of several devices are measured (Fig. 2). In this case, the wire width in the SETs is in the range from 5 nm to 15 nm. The clear Coulomb oscillation is observed at 25 K in these devices.

3. Estimation of the embedded Si height

In the PADOX process, the height of the embedded Si-wire in SET strongly depend on the length and width of the wire. The relationship of the Si height to the length and width of the wire have been revealed by AFM measurement [6]. The Si height of the devices in Fig. 2, which is estimated using the relationship, is in the range from 5 nm to 10 nm. The cross-sectional shapes of the devices are illustrated in Fig. 3.

4. SET structure and electrical property

The gate capacitance of SET strongly depends on the length of the devices, as indicated in references [2,3]. In these papers, however, because the structural parameter is a designed value and is not an actual value, the data vary widely. In this paper, for the first time, we can use measured actual dimensions of devices.

Figure 4 shows the conductance as a function of the gate voltage for the SET (No. 1 in Fig. 3). The gate capacitance Cg is derived from the peak spacing ΔVg of the conductance characteristics using the relationship $Cg=e/\Delta Vg$, where e is the elementary charge. The relationship between the measured gate capacitance and the measured wire length is shown in Fig. 5. All plots are on the same linear trend, in spite of the difference of the cross-sectional shape of the device shown in Fig. 3. The cross-sectional area estimated from the measured width and height is almost the same for all devices (Fig. 3). In this case, the gate capacitance is expressed as a function of length only. This result is confirmed by three-dimensional electromagnetic field simulation.

An effective length of the single-electron island is 23 nm shorter than the wire length, as shown in fig. 5. This situation is illustrated in figure 6. The central part of the Si wire act as the single-electron island. Both ends of the wire will act as the tunnel capacitors of SET [4]. This is the first report of the detailed structure of the Si single-electron transistors whose electrical properties have be measured.

5. Conclusions

The evaluation of the width and height of the Si island in an electrically-measured SET is performed using SEM and AFM. We estimate the effective length of the island from the fact that the gate capacitance of SET depends linearly on the length of the island in the case of the same cross-sectional area. The Si wire in SET fabricated by PADOX is divided into three regions, the SET island and two tunnel capacitors.

References

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[3] Y. Ono, et al., IEEE Trans. ED, **47** (2000) 147.
[4] S. Horiguchi et al., Jpn. J. Appl. Phys. **40** (2001) L29.
[5] M. Nagase et al., Microelectron. Eng. **41/42** (1998) 527.
[6] M. Nagase et al., Microelectron. Eng. **53** (2000) 257.

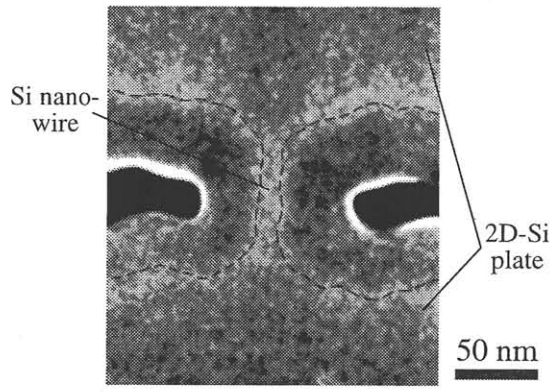

Fig. 1. SEM image of a SET. An embedded Si structure is observed through the oxide layer. SET operation of this device has been confirmed by electrical measurement at 25K. The outline of the embedded Si is represented by dotted lines. The wire length is defined as the length of the region where the width is almost constant.

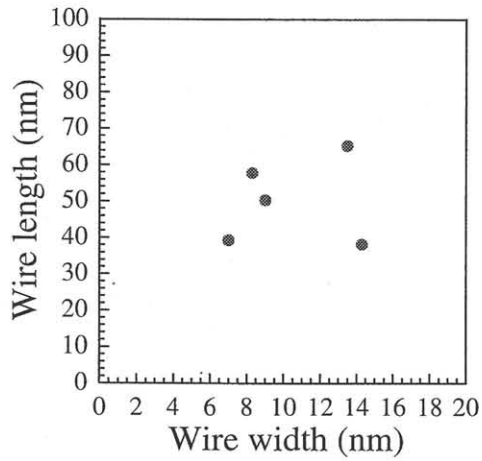

Fig. 2. Plot of critical dimensions of the SET devices. The width and length of the embedded Si wire of the devices are measured by SEM. The conductance oscillation is observed for all devices.

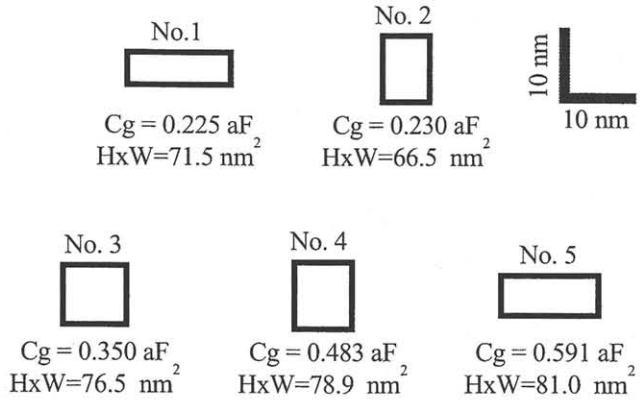

Fig. 3. The cross-sectional shapes of the Si wire in the devices shown in Fig. 2. The width (W) was measured by SEM and the height (H) was estimated from AFM results.

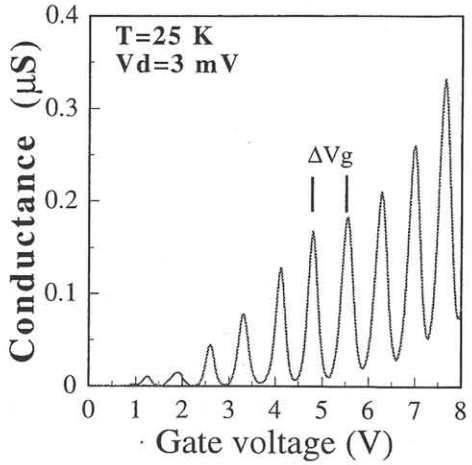

Fig. 4. The conductance characteristics of the SET (No. 1 in Fig. 3). The peak spacing is 0.711 V for this device. The gate capacitance is 0.225 aF.

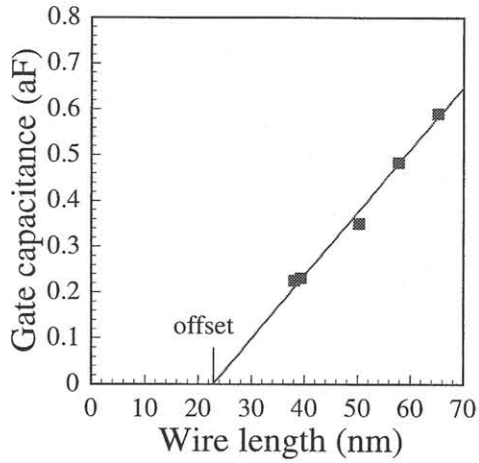

Fig. 5. Plot of the gate capacitance of SET against the wire length measured by SEM. The gate capacitance of the devices with the same cross-sectional area has a linear relationship with the wire length. The offset value in length is about 23 nm.

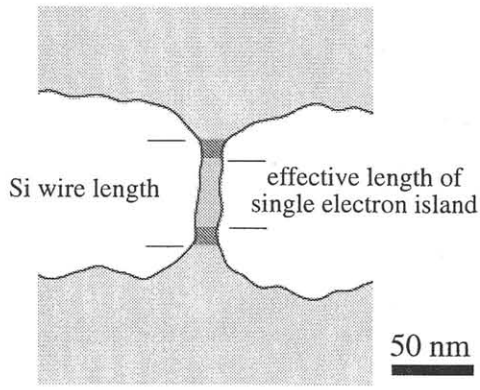

Fig. 6. Outline of the embedded Si in Fig. 1 (No. 5 in Fig. 3). The wire length of this device is 65 nm. The effective length of single electron island is estimated to be 42 nm.