Physical Modeling of Substrate Resistance in RF CMOS

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1. Introduction
Advances in deep sub-micron CMOS technology have made CMOS attractive for RF application. However, the conventional MOSFET model is not accurate when its operation frequency becomes very high [1]. An accurate RF MOSFET model requires taking account of a lot of issues [2]. Especially, the physical behaviors of the substrate resistance that affect high frequency characteristics of RF MOSFET are not well known.

In Section 2, we will propose a simple extraction method for substrate resistance of RF CMOS. In Section 3, the physical behaviors of the extracted substrate resistance were investigated by S-parameter measurement and device simulation. The results will be shown with varying drain bias, distance to body contacts, and well depth. To verify the validity of the extracted substrate resistance, we performed macro modeling using the extracted value.

2. Proposed Substrate Resistance Extraction Method
It has been reported that the substrate resistance has a very weak gate bias dependence [3]. Therefore, in this paper it is assumed that the proposed physical substrate model has no gate bias dependence, and the substrate resistance was extracted with the gate negatively biased (Vgs = -1 V). Fig. 1 shows the equivalent circuit of RF MOSFET in accumulation condition. Csb is the capacitance due to the gate charge variation for the body voltage variation [4], and Cgd and Cds are the junction capacitances, and Rsub is the substrate resistance. From Fig. 1, the real and imaginary parts of Y22, which are affected by the substrate coupling [5], were obtained as follows.

\[ \text{Re}[Y_{22}] = \alpha^2 R_{sub} \text{C}_{jd}^2 \]
\[ \text{Im}[Y_{22}] = \alpha \text{C}_{jd} \]

(1)
(2)

Therefore Cjd and Rsub can be obtained from the above equations.

3. Parameter Extraction Results
The test devices are multi-fingered n-MOSFET’s of 0.18μm CMOS technologies having unit gate width of 2.5μm, 12.5μm and 50μm. The body contacts were placed as a vertical strip along the both sides of the device and 0.45, 2.25, or 4.5 μm away from the active area. Cgd was obtained from Eq. (2) and the results are shown in Fig. 2. Cgd decreased when the drain bias increased, since the width of the depletion region became wider with higher Vds. In single finger case, Cgd was about twice those of multi-fingered devices, since the junction area is larger by factor of two. Fig. 3 shows the drain bias dependency of substrate resistance obtained from Eq. (1) for devices with different number of fingers. The substrate resistance decreases very slightly with Vds because the resistance component from the drain junction edge to body decreases due to the increase of drain depletion region width. Rsub for devices with different distance to body contacts was shown in Fig. 4. Rsub increased in proportion to the distance. Fig. 5 shows the extracted Rsub with varying well depth. In this case, S-parameters were obtained from ATLAS simulation. Rsub decreased when well depth increased. However, with well depth over 1 μm, Rsub did not vary significantly.

To verify the validity of the extracted Rsub value, we performed the full macro modeling for the device in strong inversion [6]. The BSIM3 core was augmented by R_to, Rsub, Cgdn, and Cgdo as shown in Fig. 6, with the extracted Rsub value of 11.52 Ω. Fig. 7 shows that the simulated Y-parameters have good agreement with the measured ones. Especially, the macro model for Y22 matches very well with the measurement, indicating that the extracted Rsub value is valid for different gate biases.

4. Conclusions
The substrate resistance for CMOS RF modeling was extracted when the device is at off-state. Both the junction capacitance and the substrate resistance can be obtained simultaneously from the S-parameter measurement. The substrate resistance decreased very slightly when drain bias increased, and increased in proportion to the distance to body contacts. By full macro modeling, the validity of the extraction method for different gate biases was verified.

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References
Fig. 1 The equivalent circuit of RF CMOS model when the gate is biased negatively and the device is off.

Fig. 2 The drain bias dependency of \( C_d \) for devices with different number of fingers.

Fig. 3 The drain bias dependency of substrate resistance for devices with different number of fingers.

Fig. 4 The substrate resistance for devices with different distance to body contacts.

Fig. 5 The substrate resistance with varying well depth.

Fig. 6 Macro model with the substrate resistance.

Fig. 7 The measured and modeled Y-parameters using extracted substrate resistance for the n-MOSFET biased to \( V_{gs} = 2 \text{ V} \) and \( V_{dr} = 2 \text{ V} \). The frequency range was from 100 MHz to 5 GHz. (a) \( Y_{11} \) (b) \( Y_{12} \) (c) \( Y_{21} \) (d) \( Y_{22} \)