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All Digital Wireless Modem LSI for Software Defined Radio

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1. Introduction

Digital wireless modem for short-range communication with high data rate, such as Bluetooth etc., will be most significant equipments for providing Ubiquitous Network. However, many components have been necessary to implement the wireless modem using conventional method [1]. In this paper, we have proposed a new design method for the digital wireless modem using digital LSI without antenna. The proposed design method is suitable for implementation for all digital 1-chip wireless modem. Programmability of modulation type can be obtained by simple logic structure.

2. Design method of proposed modem

The feature of proposed design method is that the clock signal has been used for carrier of modulation. Figure 1 shows the block diagram of transmitter of wireless modem using proposed design method. In transmitter, clock signal divided to more than 4 has been employed for carrier signal. The carrier frequency and symbol rate have been decided from the number of divide. QPSK (Quadrature Phase Shift Keying) has been employed for modulation. In the proposed design method, QPSK signal can be simply obtained. Figure 2 shows QPSK modulator using delay flip-flop and inverter. The input signal is the divided clock signal. Delayed singal means pi/2 shifted carrier. Inverted signal means π–shifted signal. QPSK modulation is carried out by selecting 4-type signal based on baseband digital data as listed in Table 1. Other PSK modulation, such as 8-PSK, $\pi/4$-shift QPSK, etc., can be obtained by increasing the number of D-FF. Differential coding in transmitter has been employed for simple demodulation. Figure 3 shows measurement results of QPSK modulated signal using proposed QPSK modulation method, (a) QPSK constellation, (b) spectrum of QPSK signal, (c) eye diagram, and (d) waveform of I-channel. FPGA (Field Programmable Gate Array, Xillinx Vertex V300PQ) was used for implementation. HP89410A Vector Signal Analyzer was used. In this measurement, clock frequency of LSI was 48MHz and carrier frequency is 12MHz. Data rate was 1.5Mbit/sec.

Figure 4 shows the block diagram of receiver of wireless modem using the proposed method. In the front-end of the modem, CMOS amplifier using CMOS inverter has been used as shown in Fig. 5. The received signal is converted to digital signal due to saturated operation of the CMOS inverter. In the demodulator, differential detection has been employed. Figure 6 shows differential detector using a delay line and an exclusive-or gate. Baseband signal without carrier synchronization can be obtained using this structure. Delay time of the delay line is equal to the symbol duration. After differential detection, decision of symbol is carried out. We have successfully confirmed demodulation using FPGA measurement.

3. Implementation of proposed modem

The BPSK modem using proposed design method has been designed and implemented using 0.25μm CMOS process. We used CMP (Francs) as a broker and STMicroelectronics as a foundry. Figure 7 shows the layout of designed modem. Verilog-HDL (Hardware Description Language) has been used for circuit design. Carrier frequency to be 1/4 of clock frequency and symbol rate to be 1/8 of carrier frequency has been designed. The clock frequency of 160MHz leads 40MHz carrier frequency and 5Mbit/sec deta rate.

4. Conclusion

The simple design method for digital wireless modem using CMOS LSI has been proposed. All components without antenna have been implemented by digital LSI design. In the proposed design, simple QPSK modem LSI design has been demonstrated. Programmability of modulation scheme can be obtained by simple logic structure. Proposed design method has a potential for being used to the soft ware defined radio.

References

[1] For example, Toshiba, Semiconductor System Catalog: PHS and Cordless Phone

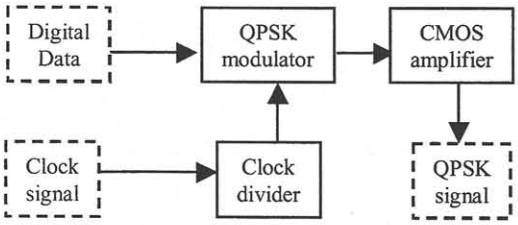

Fig. 1 Block diagram of transmitter

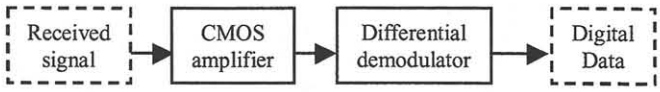

Fig. 4 Block diagram of receiver

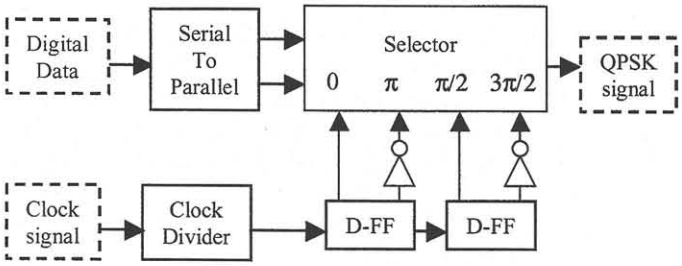

Fig. 2 Block diagram of QPSK modulator

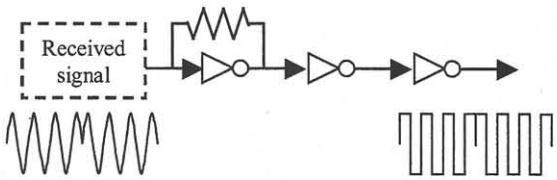

Fig. 5 CMOS amplifier

Table 1 Selection of phase

Data	Phase
00	0
01	π
10	π/2
11	3π/2

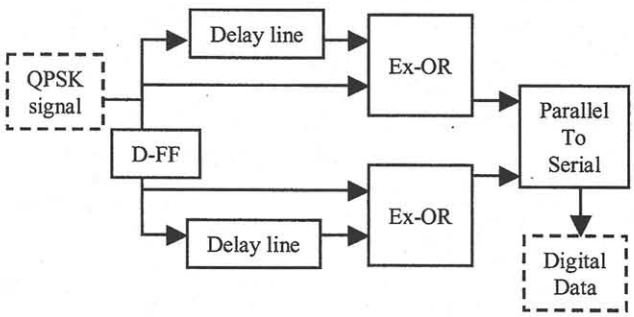

Fig. 6 Differential demodulator

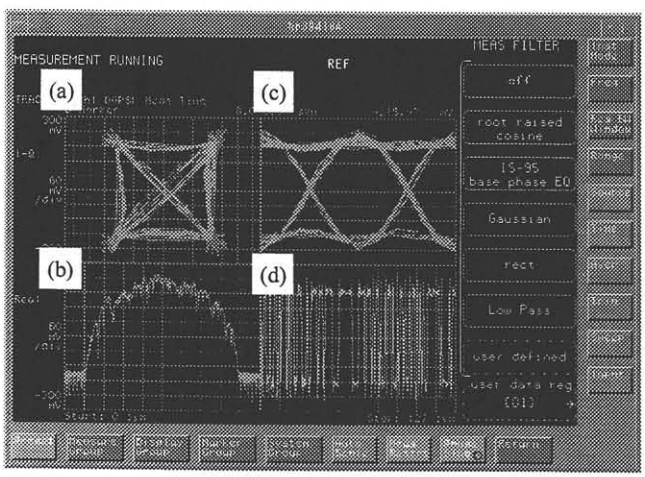

Fig. 3 Measurement results of transmitted signal (HP89410A)
(a) I-Q constellation, (b)Spectrum, (c)Eye diagram,
and (d) waveform of I-channel.

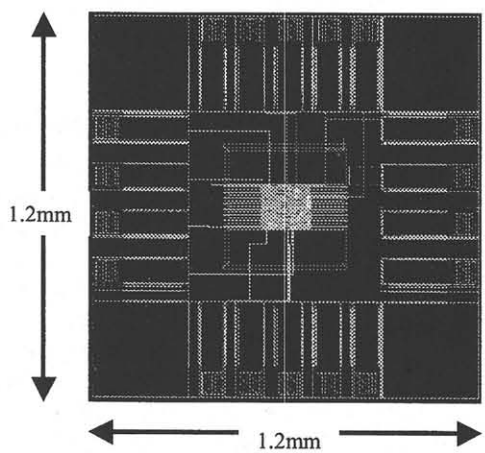

Fig. 7 Layout of the designed LSI using 0.25μm process