1. Introduction

We have developed a new bus architecture using Direct Sequence Code Division Multiple Access (DS-CDMA) technique with complete interconnection flexibility for parallel digital signal processing[1],[2]. A first prototype chip using the technique[3] demonstrated that the DS-CDMA interface is quite noise-tolerant and can transmit/receive many data simultaneously with simple interconnection protocol. However, there still remain several questions; (1) what is the maximum number of simultaneously transmitted/received data? (2) what is the most critical circuit to cause erratic data transmission?

In order to study the practical limit of the CDMA bus interface, we theoretically analyze the error probability of concurrent data transfers.

In what follows, we will theoretically calculate the error

Fig. 1 shows the schematic illustration of the proposed CDMA bus I/O interface, together with the conceptual data signal at each point. The digital bit data modulated with their respective PN code for each transmitter are output to the bus line. The receiver demodulates the signal on the bus line with the same PN code as the transmitter sending the desired data. The assignment of the same PN code for the transmitter and receiver ensures a virtual direct connection of their digital data streams because each of them has a high correlation with itself and low correlation with the others.

2. Effect of OP-AMP gain on error probability

The bus interface implemented in the prototype chip demonstrated that no bit error was detected in $1 \times 10^6$ data transfers even though the amplitude of each modulated signal was kept very small, typically 40 mV peak-to-peak on the differential bus lines. This is due to the fact that the bus interface using differential signal architecture significantly suppresses common mode noise originating from the mismatch among the devices (MOSFET, C, R) used in the transmitters and receivers except for the integrator shown in Fig.2. The aim of this work is to investigate the error probability of multiple data transfers by using a statistical approach because no erratic data transfer was detected in the previous experiments.

In the CDMA bus interface with differential signal, the most critical circuit to cause error in data transfers is the integrator in the receiver circuit shown in Fig.2. Note that the other possible cause of erratic data transfer such as substrate coupling noise, can be significantly reduced by means of layout with the greatest care. The CDMA bus line signal through the CMOS level shift circuit is demodulated with a PN code at the mixer and then integrated over a bit cycle. If there are no transmitted signals which modulated by the respective PN code at the receiver, the output of the integrator remains approximately at the mid-voltage range, because the mixer does not detect much correlation. It should be noted that concurrent multiple data communication demands the use of the integrator with high linearity.

The integrator with high linearity requires infinitely large voltage gain. However, in reality, there exists a trade-off between voltage gain, A, and bandwidth, BW of OP-AMPS. High throughput of data transfer via the CDMA bus interface can be, therefore, achieved only with reduced OP-AMP gain at a given fabrication process because of its lower Miller capacitance. The use of finite gain OP-AMP induces slight voltage difference between two inputs, meaning no more virtual short between the two terminals. This leads to non-linear integration of the differential signal.

In what follows, we will theoretically calculate the error...
probability of simultaneous data transfers which is caused by the non-linear integrator due to finite gain of the OP-AMP used in the receiver.

The output voltage, \( v_o \), of the integrator is derived from the equations given by,

\[
v_i = \frac{v_o}{A}
\]

\[
i = \frac{v_i - v_i}{R} = C \frac{d}{dt}(v_1 - v_o)
\]

where \( v_i \) and \( v_1 \) are the differential input signal and the voltage difference at the OP-AMP inputs. The convolution of pulse response functions derived from the equations above gives,

\[
v_o(T) = -Ae^{-\frac{R}{C}(t+t+A)} \sum_{n=0}^{127} \left[ e^{\frac{R}{C}(t+t+A)} \right] \frac{n!}{128^n} T
\]

where \( T \) is a bit cycle for 128-length PN codes.

3. Simulation Results

![Graph showing the distribution of output voltages for 40,000 data transfers with different combinations of PN codes. Simulations were carried out for OP-AMP gain, A, of 1600 and 100. Number of simultaneous data transferred is 10.](image)

![Graph showing the average output voltage and 5σ as a function of OP-AMP gain, A.](image)

Fig. 3: Distribution of output voltages for 40,000 data transfers with different combinations of PN codes. Simulations were carried out for OP-AMP gain, A, of 1600 and 100. Number of simultaneous data transferred is 10.

Fig. 4: Averaged output voltage and 5σ as a function of OP-AMP gain, A.

Fig. 5: Error probability as a function of the number of multiple data transmitted for the integrator with OP-AMP of A=100

4. Conclusions

We have analyzed the error probability of multiple data transfers in CDMA wired interface by using a statistical PN code generation method. A generalized form representing error probability was derived as a function of OP-AMP gain which is the most critical factor to ensure linear integration of received data. In the case of 128-length PN codes, calculated error probability was found to be as low as \( 10^{-14} \) even for 60 concurrent data transfers which corresponds to no error for 10 year's continuous operation. The very low error rate is attributed to the noise-tolerant nature of CDMA wired bus interface.

References