Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, Tokyo, 2001, pp. 410–411

P-1-6

Comprehensive Study on Reliability of Low-Temperature Poly-Si TFTs under Dynamic CMOS Operations

Yukiharu Uraoka, Hiroshi Yano, Tomoaki Hatayama and Takashi Fuyuki

Nara Institute of Science and Technology, Material Science,
Phone/Fax +81-743-72-6071 e-mail:uraoka@ms.aist-nara.ac.jp
8916-5, Takayama, Ikoma, Nara, 630-0101, Japan

1.Introduction

A low-temperature polysilicon (poly-si) process has been widely developed as a promising technology to realize mobile devices such as movies or notebook-type computers. As expanding application of poly-Si TFT-LCD, it is important to clarify the degradation mechanism in order to enhance the reliability of poly-Si TFTs under dynamic pulse. So far, we have studied the degradation for n-ch TFT under DC[1] or inverter stress[2-3]. In this work, comprehensive analysis of the degradation mechanism for p-ch and n-ch TFT were performed under CMOS operations. We have found that ON current and mobility in p-ch TFT increase under dynamic stress for the first time. Mobility change had a universal relation with the number of repetitions. A consistent model was proposed for both n-ch, p-ch TFT.

2 Sample Preparation

Crystallization of polysilicon was performed using a XeCl excimer pulse laser. Gate oxide was deposited with normal CVD method. The thickness of poly-Si was 85 nm and the effective gate oxide thickness was 95 nm. Boron and phosphorus ions were doped for the source and drain of p-ch and n-ch TFTs, respectively. Mo was used as a gate metal. The gate length and width were both 12 μm.

3. Results and Discussions

We imposed pulse stress on the gate as dynamic stress and the source and drain were grounded. The degradation of the drain current and channel mobility of n-ch and p-ch TFT as a function of time under dynamic stress is shown in Figs. 1(a) and 1(b), respectively. The magnitude of the pulse was ± 15V. The frequency of the stress pulse was 500 kHz. The drain voltage used in the measurement was 5 V. ON current and peak mobility were decreased in the n-ch TFT, however, these parameters increased in p-ch TFT.

Dependence of the degradation on frequency was examined. Degradation was monitored as the ratio of degraded mobility (μ) to initial mobility (μ_0). As shown in Fig. 2(a), the degradation of mobility was accelerated with the increase in the frequency from 0.5 kHz to 500 kHz in n-ch TFT. Degradation was replotted with the number of repetition as shown in Fig. 3(a). Independent of the frequency, the degradation exhibited a universal curve as a function of the number of repetitions. For p-ch TFT, same dependence was examined as shown in Fig.2 (b) and 3(b). With the increase of frequency, mobility change was accelerated as in the case of n-ch TFT. Almost universal curve was obtained for the number of repetition also in the n-ch TFT. These results clearly show that repetition from ON to OFF or OFF to ON enhance the degradation.

To find a dominant parameter of the pulse for the degradation of mobility, we measured the transient time dependence as shown in Figs. 4(a) and 4(b). For n-ch TFT, the degradation curve did not change for the variation of rising time, however, degradation was markedly accelerated with the decrease in the falling time. On the contrary, in the case of p-ch TFT, mobility change depended only on the pulse rise time.

Based on the results, we made a model consistent for both n-ch and p-ch TFT . Carriers (electrons for n-ch, holes for p-ch TFT) accumulated in the channel when the gate pulse was ON state (High for n-ch, Low for p-ch). These carriers move rapidly to source and drain becoming hot carriers to make electron traps at

the grain boundaries in the poly-Si film when the gate pulse changes to OFF state(Fig.5). Due to the electron traps at grain boundaries, mobility *appeared* to decrease in n-ch TFT, and to increase in p-ch TFT. The number of mobile free carriers will be different from the number estimated from the sheet charge model [4].

4.Conclusions

We have performed a comprehensive study on the reliability of low-temperature poly-Si under dynamic CMOS operations. Different from the n-ch TFT, an increase of ON current and mobility was observed in p-ch TFT for the first time. Degradation was accelerated by the repetition of pulse and depended strongly on pulse rising time. Consistent model for both types was proposed and mechanism was discussed.

Reference

[1]Y.Uraoka, et al., SSDM2000, pp446-447.

[2]Y.Uraoka, et al., Jpn. J.Appl. Phys.,Vol.39 (2000)pp. L 1209-L 1212.

[3]Y.Uraoka, et al., AMLCD2000, pp.181-184.

[4]N.S. Saks, et al., Materials Science Forum, Vols.338-342 (2000) pp.737-740.

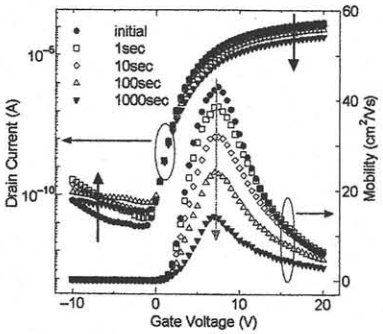

Fig.1(a) Id-Vg(n-ch TFT)

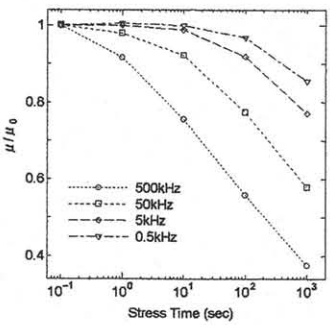

Fig.2(a) Frequency (n-ch TFT)

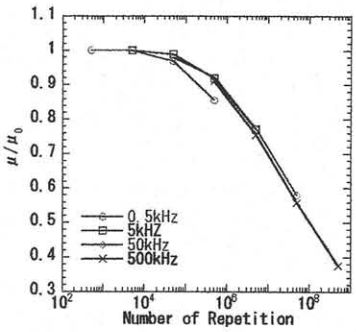

Fig.3(a) Repetition Number(n-ch TFT)

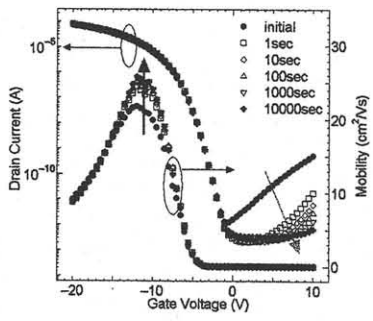

Fig.1(b) Id-Vg(p-ch TFT)

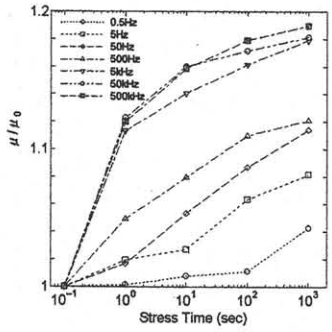

Fig.2(b) Frequency (p-ch TFT)

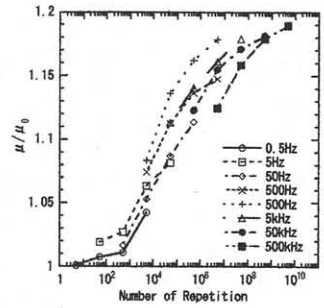

Fig.3(b) Repetition Number(p-ch TFT)

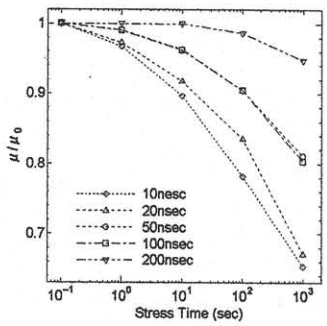

Fig.4(a) Falling Time (n-ch TFT)

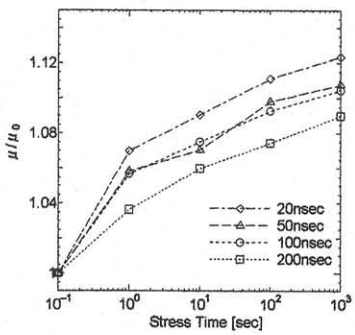

Fig.4(b) Rising Time (p-ch TFT)

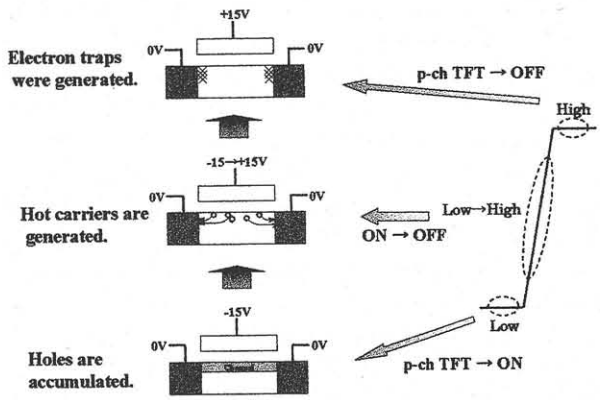

Fig.5 Degradation Model (p-ch)