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Low Temperature BST-CVD Process for the Concave-Type Capacitors Designed for Logic-Base-Embedded DRAMs

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1. Introduction

Logic-base-embedded DRAMs devices employing high-speed CPUs and other logic circuits are required for next generation digital consumer products. For these embedded DRAM devices, capacitors are incorporated after the logic transistors are in place. Therefore, capacitor fabrication thermal budgets must be low enough to be compatible with logic processes. Consequently, merging the DRAM capacitor processes (without the degrading the logic transistors) is a principal technical challenge of high-end embedded DRAM devices [1-4].

In addition to a reduced thermal budget, reduced capacitor height is preferred to provide the circuit design flexibility and improved manufacturability. To achieve the low thermal budgets capacitor processes with low stack height, BST (Barium Strontium Titanate) capacitor processes and structures have been studied [5-9]. In previous works, it has been necessary to employ relatively high temperature annealing to obtain the required BST capacitance density and charge leakage. However, on 3-D structures, high temperature anneals tend to destabilize the platinum electrodes which offer the advantage of high quality interfaces.

This paper describes electrical properties of a 0.15 μm 3-D concave-type capacitor TEG structure and process sequence with stabilized ultra-thin Pt bottom electrodes, as well as low temperature CVD-BST process. A Schematic drawing of the bottom electrode (BE) structure for the concave-type capacitor was showed in Fig.1(a), and a SEM picture of BE Pt on the 0.15 μm feature TEG structure was in Fig.2(b). A challenge with this structure is the ultra-thin (few hundred angstrom) PVD Pt bottom electrode, which tends

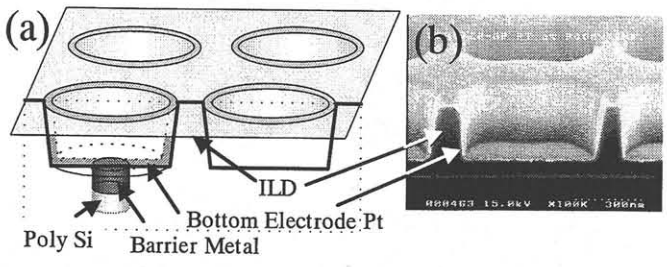

Fig. 1(a) Schematic drawing of bottom electrode structure for a concave-type capacitor. BST. BST is deposited on the structure as a high-k dielectric material. (b) A cross-sectional SEM of the TEG structure with BE Pt.

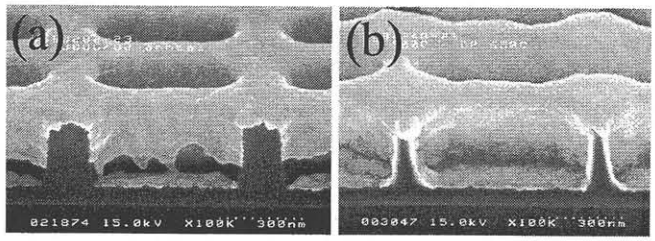

Fig. 2 SEM pictures of BE Pt after annealed in O_2 ambient. (a) without pre-anneal for stabilization (b) with H_2 stabilization anneal.

to be unstable during subsequent process steps, such as CVD BST. During the O_2 anneal, used as a simulated oxidizing ambient of CVD BST, Pt redistribution caused Pt bottom electrode defects (Fig. 2(a)). The Pt deposition process and the post-electrode anneal were optimized to improve the stability of ultra-thin Pt bottom electrode prior to the CVD-BST deposition (Fig.2(b))[10].

2. Low temperature BST process

Precursors used were $Ba(THD)_2$, $Sr(THD)_2$, $Ti(THD)_2(O\text{-}i\text{-}Pr)_2$ with THF solvent. The CVD-BST process was performed on the warm-wall 8'-inch single wafer tool with a liquid precursor delivery system. Oxygen was used as an oxidizer gas.

Fig. 3 showed that the Ti, Sr and Ba composition of CVD-BST films with the various deposition times measured with a well-calibrated XRF. Each data point indicated the average of the composition in the whole film. We found the Ti composition was higher and Ba, Sr composition was lower, as a compensation, for the thinner film as a result of the high run-to-run stability of the deposition system. We picked the oxygen flow rate as a parameter to control the Ti composition toward the thickness. In fig. 4, Ti composition dependence on the oxygen flow rate was summarized. It was clearly indicated that the Ti composition was lower with the higher oxygen flow rate and it was higher with the lower oxygen flow rate. We think that the difference in behaviors of the thickness dependence of the composition is highly related to the difference in the decomposition kinetics between Ba, Sr and Ti precursors reported [11]. The decomposition of Ba and Sr precursors are proportional to the oxygen flow rate, while the decomposition of Ti precursors is less sensitive to the oxygen partial pressure than that of Ba and Sr. It is natural to expect the surface coverage of the oxygen on the

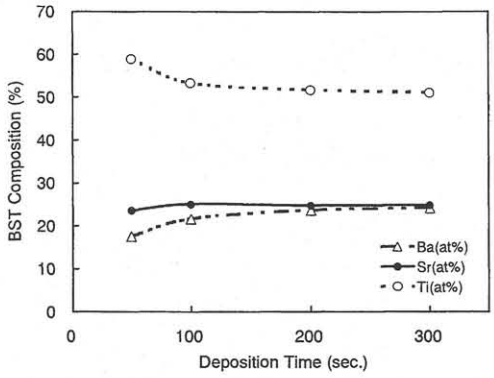

Fig. 3 Deposition time dependence of the composition of Ba, Sr, and Ti in CVD-BST films. (Ba+Sr+Ti: 100%)

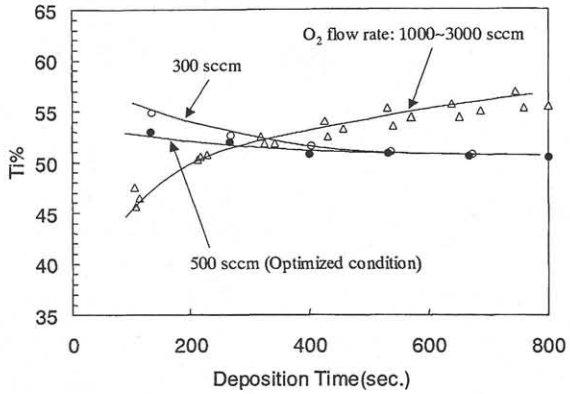

Fig.4 Deposition time dependence of Ti composition in BST films with the various oxygen flow rates.

BST film and Pt under-layer are different. Assuming the coverage of oxygen on Pt surface would be proportional to the oxygen partial pressure in the gas phase, the higher oxygen flow rate could lead higher decomposition rate of Ba and Sr precursors, and as a result, Ti composition would be lower with the higher oxygen flow rate process. We achieved the best electrical performance of the BST films with the optimized oxygen flow rate.

3. Electrical properties of CVD-BST

For comparison with 3-D structure, BST Film properties were evaluated with a planar structure. CVD BST was deposited at less than 480°C on PVD Pt/ SiO_2 substrates. The Pt top electrode was defined by shadow mask/ sputtering at room temperature, then post-top electrode anneal was performed. Fig. 5 shows the leakage at +1V of the planar capacitors measured under slow ramp rate, i.e. 1 sec. hold time, the 30 nm-thick BST film showed excellent 200mm wafer leakage performance, ~$1x10^{-8}$ A/cm^2 except some wafer edge locations, Fig.5. Capacitance density was in the range of 60 fF/μm^2 ($t_{eff\,ox}$ = 6Å) after a 700°C anneal.

To investigate the performance of low temperature BST film on 3-D topography, Pt was sputtered on wafers having 0.15 μm x 0.45 μm holes, storage node pattern, with 0.3 μm depth as shown in Fig.1. The storage node cross-section on the TEG structure showed that the low temperature BST film shows a high degree of conformality, with no observable thickness change in the 3-D structure. For the electrical properties of the BST film on 3-D patterns,

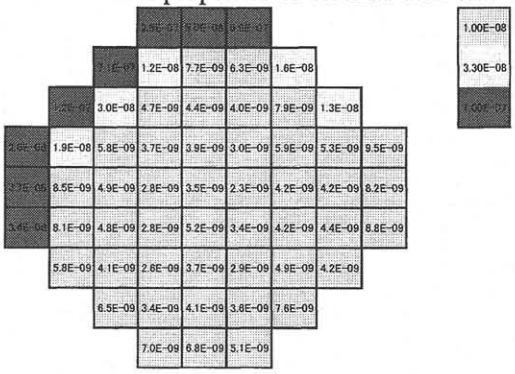

Fig. 5 Wafer map of the leakage current densities of planar capacitors

the IV curve is shown, Fig 6. The leakage current density at +1 V is, as low as, 1fA/cell averaged over a 256k array equivalent. Capacitance density of 28fF/μm^2 ($t_{eff\,ox}$ =13Å) or 12 fF/cell was achieved after annealing at less than 480°C.

4. Conclusions

Concave-type BST capacitors were fabricated using a new low temperature CVD and annealing process, lower than 480°C, and demonstrated leakage of 1 fA/cell and capacitance of 12 fF/cell for a 0.15 μm node capacitor design. This accomplishment is an important development milestone for high performance embedded DRAM planned to be implemented in the near future since it employs Pt electrodes and processing temperatures less than 480°C. Further work improving capacitor performance is suggested: optimizing post-deposition annealing conditions and stability of 3-D Pt electrodes.

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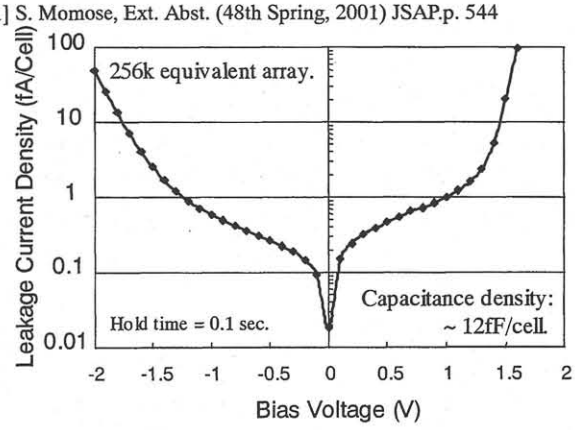

Fig. 6 Leakage current density of the 3D TEG capacitor