Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, Tokyo, 2001, pp. 4–5

PL-2 (Plenary)

Prospects of Si ULSI Devices for the Next Ten Years

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After three decades of continued growth, the microelectronic industry is facing unprecedented challenges in the next ten years. CMOS scaling, the engine that delivered higher density and performance and at the same time lower power and cost in the past, will encounter fundamental limiting factors and could be running out of steam below 50 nm dimensions. One of these factors is quantum mechanical tunneling through a few atomic layers of silicon dioxide, the miraculous material that lies at the heart of all ULSI technology. However, that does not mean scaling will come to a screeching halt. Devices will be pushed further at the expense of process complexity and chip power. For logic circuits that demand higher switching speed, a few low threshold voltage, high leakage devices with channel lengths down to perhaps 10 nm can be tolerated on the chip. Supply voltage will be slowly scaled to somewhat below 1 V, with increasing chip power. It will be expensive to push up the clock frequency near the scaling limit. Massive parallelism may become the preferred alternative to increase the processor(s) throughput.

Currently, there is a great deal of effort trying to find new material and device structures to overcome these limiting factors. Notable examples are: high-k gate dielectric, strained Si channel, SOI, and double-gate MOSFETs. While a breakthrough in any of these areas will extend the CMOS performance or the scaling limit, they cannot be regarded as a sustained source for continuing performance gains. As a matter of fact, some of these elements may not be compatible with each other and cannot be stacked up to achieve cumulative benefits.

In the next ten years, the microelectronics industry will be driven by two opposing forces at work, specialization and consolidation. For mainstream applications, like microprocessor and DRAM, optimization of particular functions leads to device specialization toward different ends of the spectra. For DRAM cells, low leakage MOSFETs with small footprints will thrive in 3-D types of structures to push cell area to the ultimate four square limit. Eventually, chip economics can only be justified by increased wafer size. In an evolution analogy, CMOS devices will diversify and specialize, each adapting to and surviving under its own environmental niche. On the other hand, the integration level and the high frequency capability of scaled CMOS devices enable new, system-on-a-chip applications. Notable examples include merged logic and DRAM, low power and RF or mixed signal chips. For these systems, some degree of device compromise is necessary in integrating a variety of heterogeneous components, including passive elements like capacitors and inductors, to deliver an overall system function. Bipolar transistors, including the SiGe variety, will continue their life in analog circuits after their extinction in the digital arena. Yield and cost issues will be a constant challenge of system-on-a-chip technologies.

While there are numerous new device concepts being explored today: single electron transistors, resonant tunneling diodes, quantum dots, carbon nano-tubes, molecular electronics, just to name a few, currently none shows the promise to replace Si CMOS in the foreseeable future. Today's ULSI technology based on Si, SiO_2, and CMOS is the ultimate outcome of the survival of the fittest. It will continue to live on for the next ten years and more.