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Strained Si- and SiGe-On-Insulator (Strained SOI and SGOI) MOSFETs as New Device Options for High Performance CMOS

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1. Introduction

MOSFET with a high mobility channel is an attractive device structure, which leads to reduction in supply voltage with maintaining the high circuit performance. From this viewpoint, a strained-Si channel is promising for CMOS application [1], because of the high electron and hole mobility. As seen in Fig. 1, the enhancement factors of electron and hole mobility, defined by the ratio of mobility in strained-Si MOSFETs to that in conventional Si MOSFETs, are roughly twice. In addition, a strained-SiGe channel structure is also suitable for p-MOSFETs, because of the high hole mobility. Thus, these MOS devices utilizing Si/SiGe heterostructures can provide various options in advanced CMOS configurations.

However, strained Si/SiGe CMOS on Si bulk substrates have the same obstacles as conventional Si CMOS, such as junction capacitance, junction leakage current, short channel effects and so on. Therefore, we have proposed strained-Si/ SiGe-on-Insulator MOSFETs to overcome these problems [2, 3]. This paper reports the recent progress on these devices and the fabrication processes.

2. Advantages of Strained-Si-On-Insulator (Strained-SOI) MOSFETs

Fig.2 shows the typical device structure of strained-SOI MOSFETs, where strained-Si/relaxed SiGe layered films are formed on a buried insulating layer [2]. Particularly, by adopting fully-depleted (FD) structure having a thin SOI layer, strained-SOI MOSFETs become more attractive for sub-100 nm node CMOS. The advantages are listed as follows [3]; (1) high mobility of strained Si combined with lower impurity scattering and lower E_{eff} (2) low junction capacitance and low junction leakage current (3) suppression of short channel effects (4) reduction in statistical variation of V_{th} (5) suppression of floating body effects due to hole current flow through SiGe pn-junction in the source region (6) no need of thick graded-SiGe buffer layers (7) low dislocation density in relaxed SiGe due to slip at the interface between SiGe and buried oxide.

3. Fabrication and Electrical Characteristics of Strained-SOI MOSFETs

The most important process in the fabrication of strained-SOI MOSFETs is the preparation of thin and relaxed SiGe-On-Insulator (SGOI) substrates with minimal dislocation density. The main concept of our original approach to the SGOI fabrication [4] is summarized in Fig. 3. When SOI substrates including SiGe layers are oxidized at high temperatures, Ge atoms are rejected from the oxidized layer during the oxidation. On the other hand, the diffusion of Ge atoms towards the substrate is blocked by the buried oxide. As a result, as the oxidation proceeds, Ge atoms are condensed into the remaining SiGe layer. This technique is applicable to a variety of substrates including bulk and SOI substrates with SiGe films. We have successfully fabricated strained-SOI MOSFETs on both types of substrates. Using SGOI substrates made by the combination of SIMOX and oxidation, the operation of strained-SOI CMOS and CMOS ring oscillators have been demonstrated, for the first time [5]. The mobility behaviors are shown in Fig. 4. The mobility enhancement of 1.85 and 1.53 has been obtained for n- and p-MOS, respectively, at Ge content of 25 %. It was also found from the waveform of 101-stage ring oscillators (Fig. 5) that strained-SOI CMOS is 70 % faster at V_{dd} of 1.5 V and 30 % faster at V_{dd} of 2.5 V than conventional SOI CMOS.

Also, ultrathin strained-SOI structures with the total thickness of 21 nm and high Ge content (x>50%) have been fabricated by oxidizing $Si_{0.92}Ge_{0.08}$ on SOI substrates and re-growing strained-Si films [6]. Recently, the successful operation of strained-SOI n-MOS, using SGOI substrates fabricated by oxidizing SiGe on SOI substrates, has been achieved with the mobility enhancement of 1.67 under the Ge content of 23 % [7].

4. Strained-SiGe-On-Insulator (SGOI) MOSFETs

The same oxidation technique can also provide substrates for strained-SGOI p-MOSFETs (Fig. 6). The hole mobility enhancement of 2.3 times as high as the universal mobility has been obtained for surface channel p-MOS with a 19 nm-thick $Si_{0.58}Ge_{0.42}$ channel layer with no Si cap, meaning the high crystal quality of the fabricated SGOI substrates [8].

5. Conclusions

We have proposed and demonstrated high performance strained-SOI and SGOI MOSFETs. It is strongly expected that these MOSFETs based on Si/SiGe heterostructures can provide new device options to sub-100 nm CMOS technology with high performance/low power consumption.

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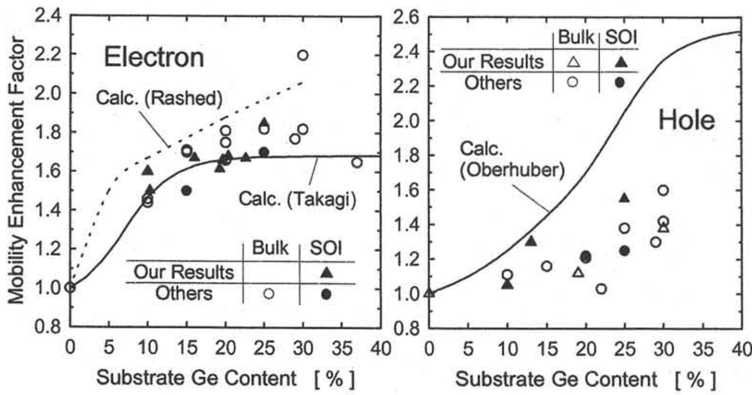

Fig. 1 Enhancement factor of electron and hole mobility in strained-Si and strained-SOI MOSFETs against the universal mobility as a function of Ge content in relaxed SiGe substrates. Curves show the theoretical results [9-11].

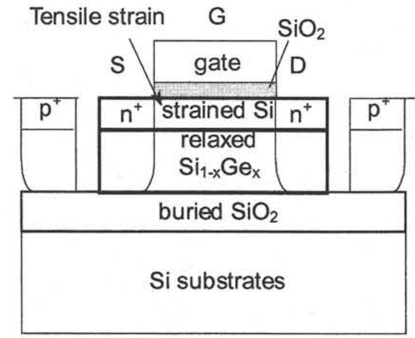

Fig. 2 Cross section of typical device structure of strained- SOI MOSFETs.

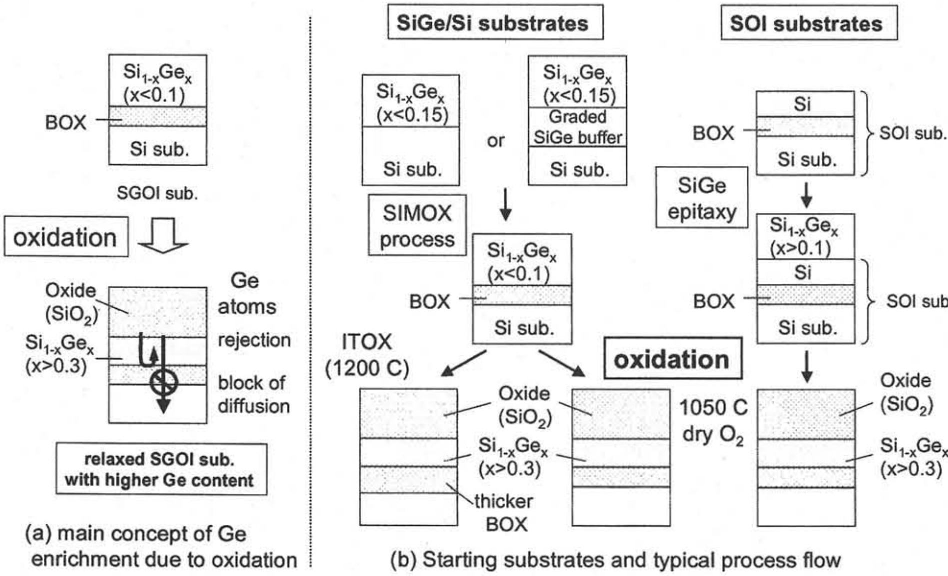

Fig. 3 Schematic diagrams of (a) main concept of the fabrication technique to obtain SGOI substrates with high Ge content by oxidizing SGOI substrates with low Ge content, called Ge condensation technique
(b) typical process flows using bulk Si and SOI substrates.

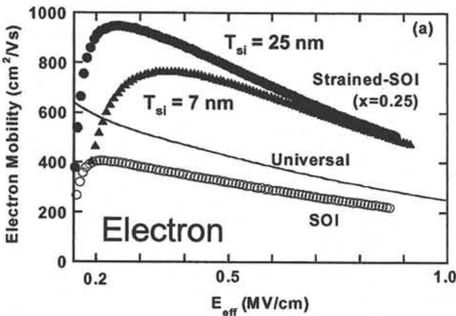

Fig. 4 Effective electron and hole mobility in strained-SOI CMOS as a function of E_{eff}. The universal mobility is also shown. Two types of substrates with strained-Si thickness of 25 and 7 nm were used for CMOS fabrications. The Ge content is 25 %.

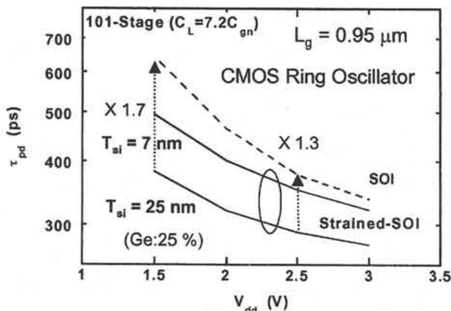

Fig. 5 Delay time of CMOS ring oscillators

Fig. 6 Schematic diagram of surface-channel SGOI p-MOSFET structure

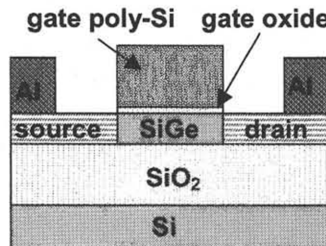

Fig. 7 Effective hole mobility of SGOI p-MOSFET as a function of E_{eff}.