Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, Nagoya, 2002, pp. 10-11

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Enhanced performance from SiGe pMOSFETs Fabricated on Novel SiGe Virtual Substrates Grown on 10μm x 10μm Si Pillars.

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1. Introduction

We present silicon germanium pMOSFETs fabricated on silicon germanium virtual substrates. These novel virtual substrates were grown by MBE on 10μmx10μm silicon pillars formed by dry etching trenches into the original silicon substrate. Relaxation of the SiGe virtual substrate is promoted by the pillars, and this in turn reduces cross hatch and increases the wafer surface planarity. The devices have 5nm silicon germanium channel with a germanium content of 70%. This is grown on top of a relaxed virtual substrate with a germanium content of 30%. A 2nm silicon cap separates the SiGe channel from the gate oxide. SiGe devices have saturation drain current up to 65% higher than their conventional silicon counterparts.

MOSFETs with improved channel carrier mobility and saturation drain current have been demonstrated with the use of high carrier mobility strained layers grown on top of relaxed silicon germanium virtual substrates [1-5]. However, the use of such a technique is complicated by the formation of cross hatch patterns on the surface of the relaxed SiGe virtual substrates caused by the stress fields in the SiGe virtual substrate as it adapts to the different lattice constant of the silicon substrate wafer [6]. Reducing the lateral dimensions of the growth zone has been shown to reduce or eliminate cross hatch. This is achieved by growing such layers on top of microscopic pillars etched into the original silicon wafer substrate [6-7], as shown in the TEM picture in figure 1. In this paper we report on novel SiGe pMOSFET devices fabricated on top of such substrates.

2. Device Fabrication

Virtual substrates were fabricated by first etching 2.5μm deep trenches into the silicon substrate wafer to define the perimeter of 10μm x 10μm silicon pillars. These pillars were then implanted with phosphorus and this dopant was activated by RTP. Undoped Silicon germanium layers were then grown on top of the pillars by solid source MBE. Layer growth started with a 1μm thick linearly graded buffer layer, graded between 0% and 30% Ge. On top of this layer a 250nm relaxed $Si_{0.7}Ge_{0.3}$ buffer layer was grown, followed by a 5nm $Si_{0.3}Ge_{0.7}$ channel and a 2nm $Si_{0.7}Ge_{0.3}$ cap. The layer structure was completed with a Si cap, some of which was consumed during gate oxidation, to give a final thickness of 2nm. A diagram of this layer structure is shown in figure 2. After MBE layer growth a 500nm layer of LTO was deposited on the wafer to form the field oxide. Active area windows were wet etched into this oxide to expose the tops of the pillars so that devices could be fabricated on top of the pillars. The gate oxide was 5nm thick, and the insitu doped polysilicon gate electrode 200nm thick. Source/ drain extensions and HDD were implanted with BF_2, and these were activated by anneal at 800C for 30 minutes. Devices were completed with a conventional back end of BPSG ILD and Ti/AlSi metallization. Silicon reference devices were also fabricated with a MBE grown substrate layer of undoped silicon grown on top of similar pillars.

3. Electrical Results

Vd vs. Id curves for 2μm Si and SiGe devices are shown in figure 3, Vg vs. Id curves for these devices are shown in figure 4 and effective hole mobility is shown in figure 5. Threshold voltage for the 2μm SiGe device is 0.38V, compared to 0.05V for the silicon device due to the valance band offset of the SiGe buried channel. Drain current at Vd=-2.5V and Vg-Vt=-2.5V was -114μA/μm width for 2μm SiGe device which is 65% higher than the -69μA/μm of the Si device. Maximum effective hole mobility of the silicon germanium devices is $156cm^2V^{-1}s^{-1}$, the mobility of the silicon reference device of $94.6cm^2V^{-1}s^{-1}$. Improved saturation drain current, effective hole mobility, and transconductance in SiGe devices with channel lengths down to 0.4μm are shown in figures 6 to 8.

4. Conclusion

SiGe MOSFETs have been fabricated on novel SiGe virtual substrates. SiGe virtual substrates are grown on top of microscopic pillars which promote the relaxation of the virtual substrate and reduces cross hatch on the wafer surface. Device characteristics show an increase in SiGe saturation drain current of up to 65% compared to silicon counterparts. This, as well as improvements in channel carrier mobility and transconductance is due to the higher carrier mobility of the 5nm thick strained $Si_{0.3}Ge_{0.7}$ channel.

References

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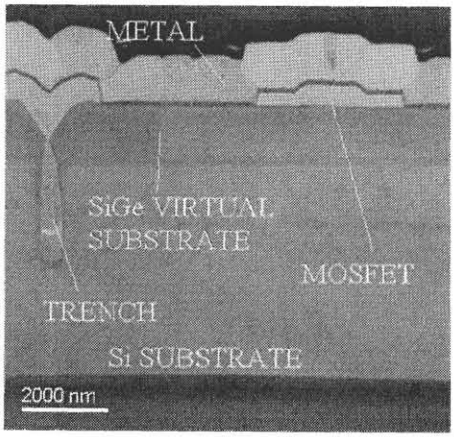

Fig 1. Cross sectional TEM picture of a MOSFET gate fabricated on top of a SiGe virtual substrate. The pillar is created by etching trenches into the original silicon substrate around the perimeter of the trench.

5nm Gate Oxide
2nm Si Cap
2nm $Si_{0.7}Ge_{0.3}$ Cap
5nm $Si_{0.3}Ge_{0.7}$ Channel
250nm $Si_{0.7}Ge_{0.3}$ Relaxed Buffer Layer
1μm Si_1Ge_0 to $Si_{0.7}Ge_{0.3}$ Graded Buffer Layer

Fig 2. Diagram of the silicon germanium layer structure in the substrate.

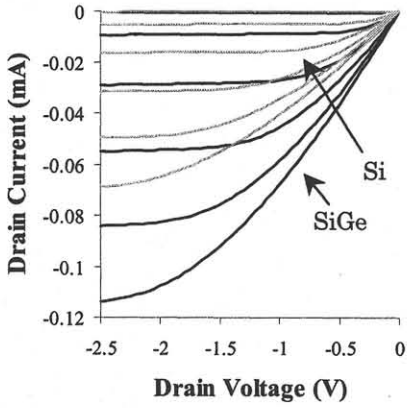

Fig 3. Drain voltage vs. drain current curves of 2μm Si and SiGe pMOSFETs The gate voltage for these curves range from the threshold voltage (Vt) to -2.5V+Vt in- 0.5V steps.

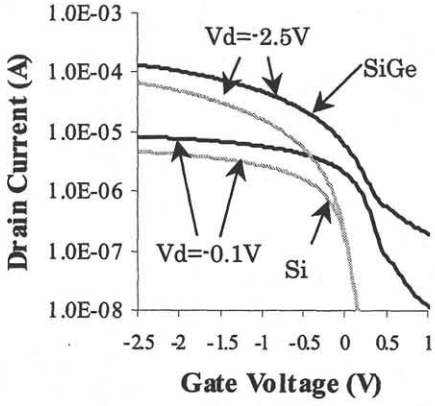

Fig 4. Gate voltage vs. drain current curves of 2μm Si and SiGe pMOSFETs.

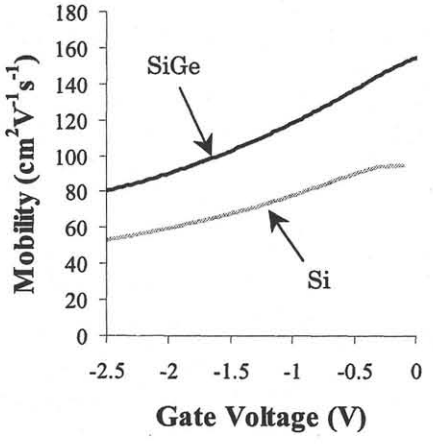

Fig 5. Effective hole mobility measured at Vd=-100mV for 2μm Si and SiGe pMOSFETs.

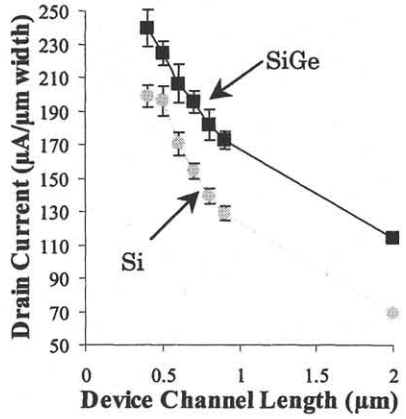

Fig 7. Saturation drain current of Si and SiGe pMOSFETs measured at Vd=-2.5V, Vg=Vt-2.5V, plotted as a function of channel length.

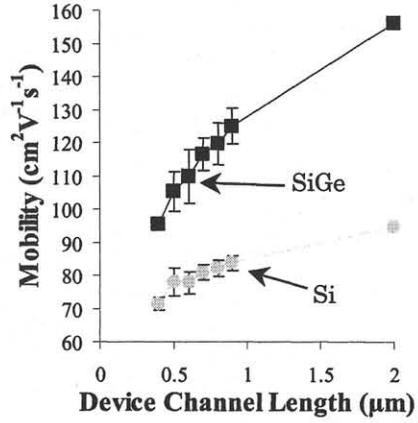

Fig 6. Effective hole mobility for Si and SiGe pMOSFETs plotted as a function of channel length.

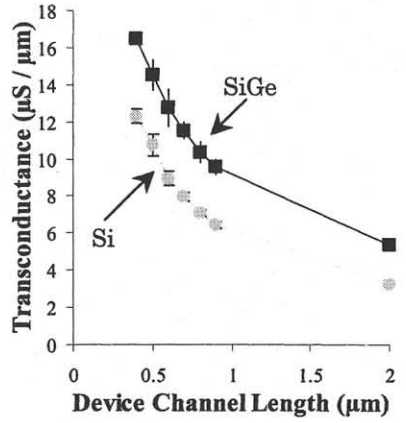

Fig 8. Device transconductance of Si and SiGe pMOSFETs measured at Vd=-100mV, plotted as a function of channel length.