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Novel Strained-Si Substrate Technology for Transistor Performance Enhancement

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1. Introduction

Strained-Si channel transistors offer significant performance enhancement. However, most designs based on bulk-Si substrates utilize thick SiGe buffer layers or complex multi-layer structures for the introduction of tensile strain in the Si channel and might not be easily or economically integrated into a conventional CMOS process [1]. Various methods to implement strained-Si substrates based on silicon-on-insulator (SOI) wafers have also been demonstrated [2]-[3], but they suffer from an inherent high cost and process complexity. In this paper, we present a new, inexpensive, and manufacturable strained-Si substrate technology based on bulk-Si substrate, and demonstrate significant enhancement in transistor performance.

2. Strained-silicon Substrate Technology

The implementation of a tensile strained-Si transistor requires a relaxed SiGe substrate with low dislocation density and surface roughness. Most techniques to achieve relaxed SiGe substrate rely on dislocation-induced relief of elastic strain and their confinement using dislocation filters such as graded layers. In this work, we make use of a strained-Si on $Si_{1-x}Ge_x$/Si/$Si_{1-y}Ge_y$/bulk-Si multi-layer structure where dislocation formation is favored or confined around the bottom $Si_{1-y}Ge_y$ layer. Strain-relieving glide of threading dislocation is facilitated during the initial epitaxial growth, preventing accumulation of the mismatch strain. When the topmost $Si_{1-x}Ge_x$ layer is grown to a thickness above 1000 Å, nucleation of additional dislocations during growth is suppressed as the threading dislocations in the initial 1000 Å can relieve strain. This successful confinement of dislocations is evident from the cross-sectional TEM of the substrate (Fig. 1). It is also evident that most dislocations propagate downwards to the bulk-Si substrate, a phenomenon which is important for the achievement of low defect density at the surface. Our defect density of 10^3-10^4 cm^{-2} is among the best achieved compared with existing technologies (Fig. 2). Raman spectroscopy confirms the existence of tensile strain in the topmost silicon channel layer (Fig. 3). Atomic force microscopy (AFM) (Fig. 4) reveals that the strained Si surface has an excellent surface roughness (11 Å), better than that of a conventional graded SiGe buffer substrate (> 15 Å).

3. Device Fabrication and Results

Surface channel strained-Si N- and P-MOSFETs were fabricated on substrates with relaxed $Si_{0.8}Ge_{0.2}$ using a novel process with a single lithography step. After SiO_2 gate dielectric (17 Å) formation, poly-Si gate was deposited and etched. This was followed by source/drain extension and halo implants, spacer formation, source/drain implants, dopant activation anneal, and Co salicidation to complete the device fabrication. Control devices were fabricated on a bulk Si substrate. Fig. 5 shows the excellent subthreshold behavior and low off-state leakage of the strained Si devices. The strained-Si NMOSFET shows 35% higher drive current compared to the bulk Si control device for the same gate overdrive V_{GS} - V_{TH}, as depicted in Fig. 6. This is due to the preferential occupation of electrons in the Δ_2 conduction band valleys with reduced effective mass and higher mobility in strained-Si. Significant electron mobility enhancement is observed (Fig. 7). Hole mobility is apparently unchanged (Fig. 8), and the performance of P-channel devices is comparable with that of the control devices. Fig. 9 shows that the strained-Si and bulk Si devices with the same gate oxide thickness have comparable gate leakage current densities.

4. Conclusion

A new low-cost and manufacturable strained-Si substrate technology with low defect density and surface roughness is reported. Significant NMOS drive current enhancement is demonstrated. The adoption of strained-Si is a promising approach for improving CMOS performance.

Acknowledgments

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References

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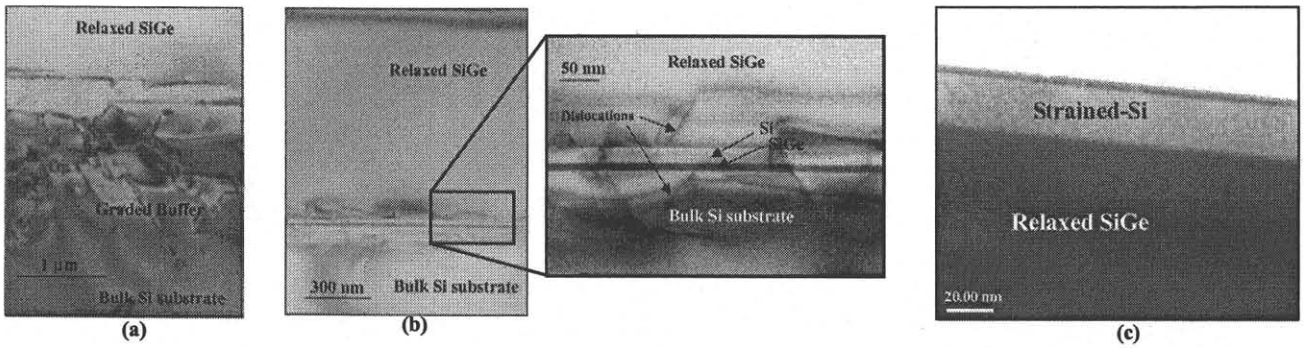

Fig. 1. Cross-sectional TEM of (a) conventional graded SiGe buffer and (b) relaxed-SiGe/Si/SiGe/bulk-Si substrate, both grown at TSMC. Downward propagation of dislocation into the substrate is evident in (b). This phenomenon is important for achieving low defect density at the surface of the (c) strained-Si layer grown on the relaxed SiGe layer.

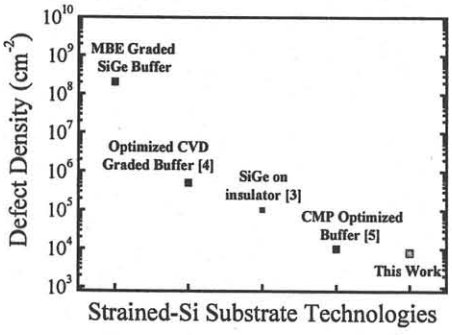

Fig. 2. Comparison of the defect density of TSMC's strained-Si substrate and existing technologies. Low defect density of 10^3-10^4 cm^{-2} is achieved, comparable with the best reported data.

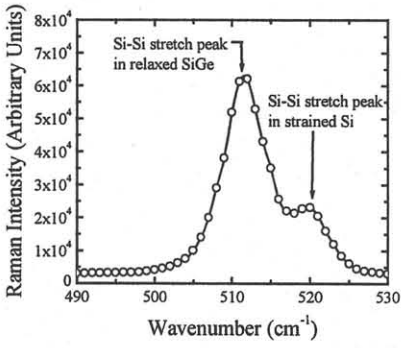

Fig. 3. Analysis using Raman Spectroscopy confirms the existence of tensile strain in the silicon channel layer.

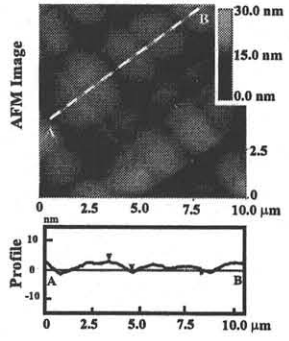

Fig. 4. Atomic Force Microscopy of the strained silicon surface reveals excellent surface roughness of ~11 Å.

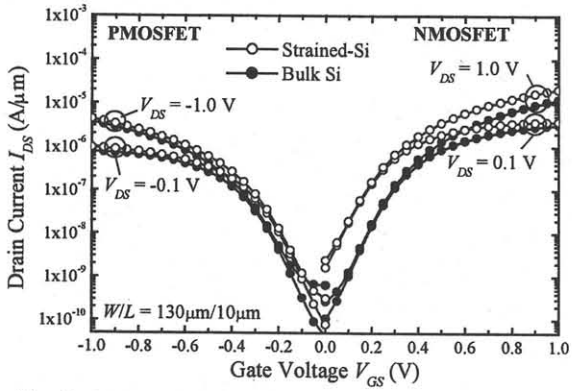

Fig. 5. I_{DS}-V_{GS} characteristics of N- and P-channel transistors showing excellent subthreshold behavior and off-state leakage.

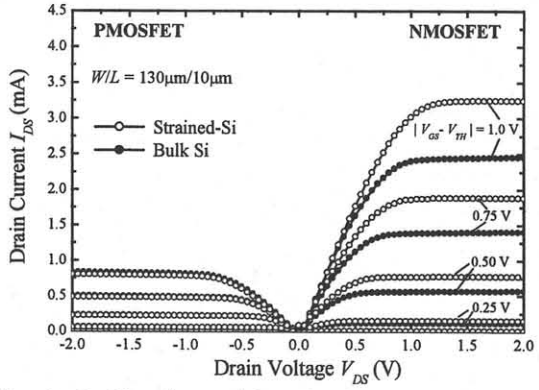

Fig. 6. I_{DS}-V_{DS} characteristics showing 35% drive current enhancement in strained-Si NMOSFETs. $|V_{GS} - V_{TH}|$ varies from 0 to 1 V in 0.25 V increments.

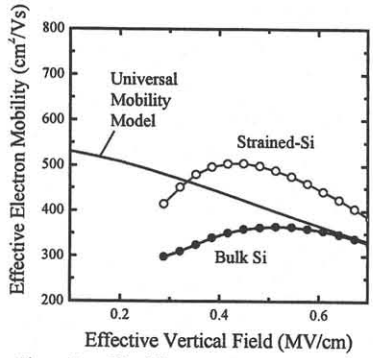

Fig. 7. Significant electron mobility enhancement is achieved.

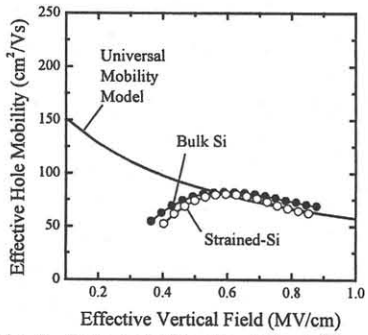

Fig. 8. Hole mobilities in strained-Si and control devices are comparable.

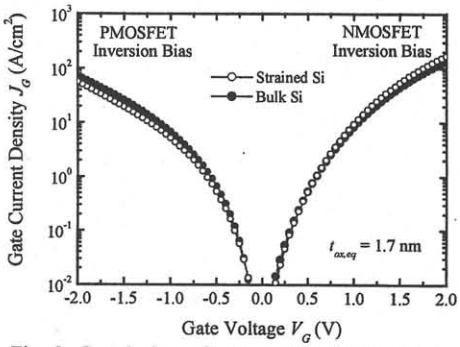

Fig. 9. Gate leakage for N- and P-MOSFETs are comparable for strained-Si and control devices.