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Simulation of Intrinsic Fluctuations in Decanano MOSFETs: Present Status and Future Challenges

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1. Introduction

In the past couple of years MOSFETs have reached deep decananometre (sub 50 nm) dimensions with 40-50 nm physical gate length devices available now in the 90 nm technology node [1, 2], 35 nm transistors ready for mass production in $2-3$ years time [3] and 10 nm MOSFETs with conventional architecture demonstrated in a research environment [4]. As it could be seen from Figures 1-3 MOSFETs are becoming truly atomic scale devices. Intrinsic parameter fluctuations play an increasingly important role in such devices at a time when the fluctuation margins shrink due to reduction in supply voltage and increased transistors count per chip. For example, in a ten billion transistors chip thousands of transistors are expected to have a 6σ deviation in their parameters. With 0.85 V supply voltage and expected σV_T in the range of $20-30$ mV this translates to thousands of transistors with threshold voltage of zero or half the supply voltage, which might affect not only the speed but also the functionality of the corresponding circuits. Various sources of intrinsic parameters fluctuations have been studied using numerical simulations including random discrete dopants [5, 6] line edge roughness (LER) [7, 8] and oxide thickness variation [9]. Such simulations studies require accurate yet efficient models and 3D statistical simulation tools.

2. Simulation challenges

The challenge is to develop simulation methods and tools for the simulation of atomic scale devices that will bridge the gap between the present continuous classical and quantum semiconductor device simulation approaches and the *ab-initio* methods of quantum chemistry in describing, with progressive accuracy, phenomena related to

(i) Discreteness of charge and matter at an individual dopant and carrier level;

(ii) Quantum transport at the atomic scale.

(iii) Statistical intrinsic parameter fluctuations associated with random dopants, imperfect interfaces, boundaries and contacts in ultrasmall devices.

It is clear that in nano-scale devices with critical dimensions measured in tens or single lattice spacings, the granularity of charge and matter has to be properly accounted for. The simulation paradigm shifts from techniques considering the device as a continuous media and based on the solution of the Boltzmann Transport Equation (BTE) to near first-principles quantum approaches which consider the device as a collection of atoms or ions and calculate the current based on the individual and collective motion of charges.

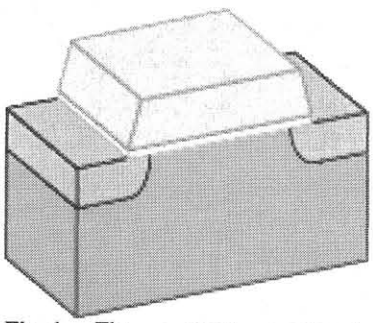

Fig. 1 The current approach to semiconductor device simulation assumes continuous ionised dopant charge and smooth boundaries and interfaces.

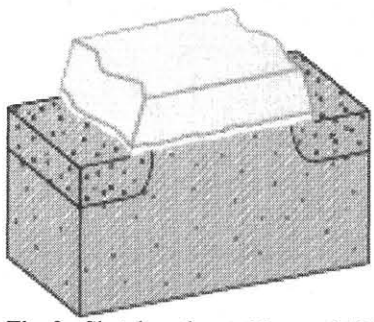

Fig. 2 Sketch of a 20 nm MOSFET expected in mass production before 2010. There are less than 50 Si atoms along channel. Random discrete dopants, atomic scale interface roughness and line edge roughness introduce significant parameter. fluctuations.

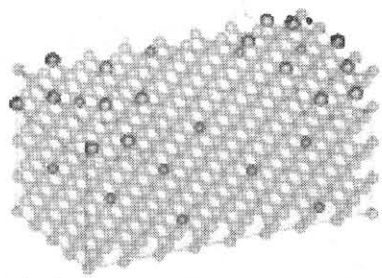

Fig. 3 Sketch of a 4 nm MOSFET expected in mass production in 2020. There are less than 10 Si atoms along the channel. The size of the device becomes smaller than the size of biologically important molecules like ionic channels.

It must be noted that the traditional ensemble Monte Carlo simulation approach does not meet this criteria, being simply a statistical technique for solving the continuous BTE. Complex problems associated with random variation in the impurity and surface limited mobility, interface states and localised tunnelling through a few atomic layers of oxide, noise and plasma coupling between the individual carriers in the channel and the adjacent regions have to be treated at an atomistic level. This has to be complemented with atomic scale process modelling which will provide atomic resolution description of the device structure.

3. State-of-art

The state-of-art 'atomistic' device simulation studies of intrinsic fluctuations introduced by discreteness of charge and atomicity of matter are still based on the drift-diffusion simulation approach [5, 6, 7, 8, 9] which is the only viable option at present for 3D simulations on statistical scale. Only recently quantum mechanical corrections have been introduced in the 'atomistic' simulations based on the density gradient algorithms [6]. The density gradient approach can be successfully calibrated in respect not only of inversion layer quantisation effects but also, as shown in Fig. 4 in respect of source-to-drain tunnelling.

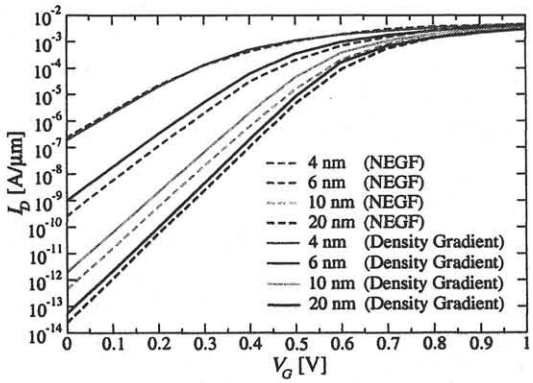

Fig. 4: I_D-V_G characteristics obtained from non-equilibrium Gereen's functions simulations and calibrated DG simulations for double gate MOSFETs with gate lengths ranging from 20nm down to 4nm. V_D= 1V and V_G applied to both top and bottom gate contacts.

We have applied recently this approach to study intrinsic parameter fluctuation in sub 10 nm double gate MOSFETs. The importance of the atomic scale effects in such devices, which are expected to supersede the conventional MOSFETs, becomes clear from the Photoshop impression in Fig. 5 constructed from SEM micrographs of real interfaces. Random dopants in the source/drain regions, stray charges in the silicon channel, interface roughness, an LER will introduce parameter fluctuations on a massive scale in these, supposedly, fluctuation resistant devices. Fig. 6 illustrated the standard deviation in the threshold voltage induced by unavoidable random dopants in the source/drain regions

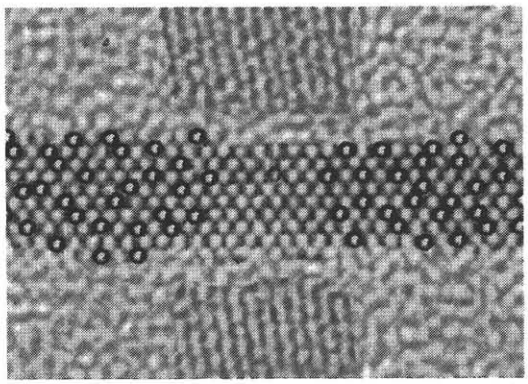

Fig.5: Impression of a 4 nm gate length double gate MOSFET illustrating the various sources of intrinsic parameter fluctuations.

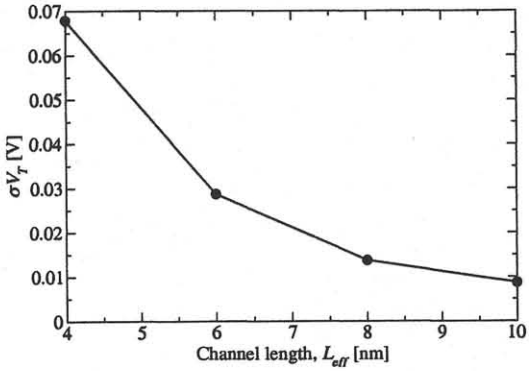

Fig.6: Standard deviation in threshold voltage, σV_T, due to random discrete dopants in the source and drain of double gate MOSFETs with different channel lengths.

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