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Modeling and Analysis of Gate Line Edge Roughness Effect on CMOS Scaling Towards Deep Nanoscale Gate Length

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1. Introduction

The line edge roughness (LER) of photoresist patterns may be a serious limiting factor in CMOS scaling into the nanometer regime [1] [2], because the current state-of-the-art edge roughness of the gate poly lines is of order of several nanometers (> ~5 nm), leading to significant performance fluctuations in the devices with extremely small dimensions. In this work, we have employed two-dimensional simulation approach and the simplified physical modeling for on- and off-state current variations to understand and analyze the impact of statistical gate line edge roughness on : (1) the device parameter fluctuations, (2) the short channel performance associated with minimum gate length, (3) conventional effective channel length extraction methods such as Shift & Ratio method, and (4) the future CMOS technology generation.

2. Modeling and Simulation Approach

In order to evaluate LER effect on the device current behavior, the total gate width (W) is divided into N segments with a certain width (ΔW) indicating the spatial frequency of W/ΔW which is attributed to process conditions. Each segment has a different gate length obeying Gaussian statistics with a specific standard deviation of line edge fluctuation (Fig 1). The mean value of N gate lengths which form a gate poly line of one transistor is adjusted to be equal to the given nominal gate length, L_g. Two-dimensional (2-D) device simulations using MEDICI are performed to obtain the device current characteristics of each segment of which gate lengths are randomly generated using Gaussian distribution. The sum of N current segments yields the current characteristics of one transistor having specified LER. In this modeling approach, the non-uniform current flow effects such as current crowding near the source/drain extension junction due to non-uniform junction edge alignment between neighborhood segments are neglected, so that we can estimate minimum performance fluctuation trends with the assumption of identical standard deviations of the device parameters with real devices.

3. Gate Line Edge Roughness Effect

Device Parameters and Performance Fluctuation

From the I_{ds}-V_{gs} characteristics of 30 devices with different gate line edge distribution with σ_{Lg} = 5 nm, the LER effect is found to be very severe in deep nano-scale gate length devices (Fig. 2). Specifically, LER causes the exponential fluctuation dependence behavior of the subthreshold current due to short channel effect (SCE) induced saturation threshold voltage reduction, resulting in the significant increase of off-leakage current (I_{off}). The important device parameters such as threshold voltages, subthreshold swing (S), I_{off} and I_{sat} are investigated as a function of process parameters such as σ_{Lg}, spatial frequency, and minimum gate length. More than 100 mV of high saturation voltage uncertainty (σ_{Vthsat}) and ~ 10 times increased I_{off} and its increased variance will be resulted in the 35 nm gate length technology, if the current LER is employed and more severe as devices are narrower (lower special frequency) (Fig. 3~5). The simplified physical expressions are developed and indicate that the key parameters determining I_{off} fluctuation are the spatial frequency, the ratio of gate length variation ($\Delta L_{gi}/L_g$), and the saturation threshold voltage deviation ($\Delta V_{thsat,i}$).

Impact on Channel Length Extraction Method

The conventional channel length extraction methods based on the linear drain current measurement such as Shift & Ratio method are also affected by LER effect. The extracted gate lengths are found to be shorter than the real average gate lengths and much shorter as σ_{Lg} increases or $L_{g,min}$ decreases, since the linear drain current (I_{lin}) also decreases in proportion to gate LER due to negative V_{thlin} shift (Fig. 6). The impact of LER on the extracted effective gate length ($L_{g,eff}$) can be analyzed with simple model.

Impact on Nanometer CMOS Scaling

On the basis of this modeling and characterization methodology, we have investigated LER effect on the nano-scale CMOS technology generation using σ_{Vth} projection of ITRS to provide a guideline for the future process technology improvement. It is suggested that less than 2 ~ 3 nm of LER is required to reduce I_{off} and V_{th} fluctuation for a successful CMOS scaling into deep nano-scale physical gate length regime (Fig. 7).

4. Conclusions

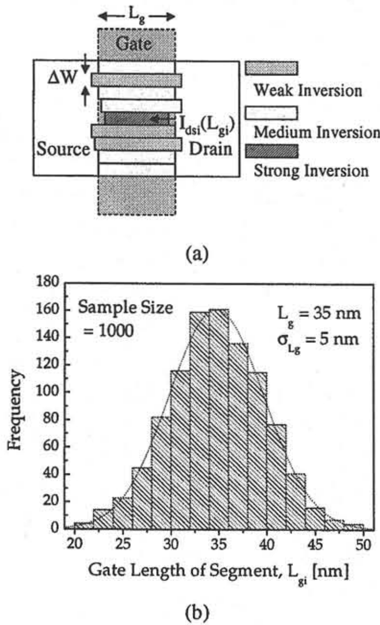
Through the simple modeling and simulation approach for the gate line edge effect on the device performance and fluctuation, the unacceptably large I_{off} and V_{thsat} uncertainty due to LER effect are predicted in deep nano-scale CMOS generation. The substantially reduced gate LER by accelerated progress in lithography and pattern transfer

process technology will be highly required to meet ITRS requirement and successful CMOS scaling.

References

[1] P Oldiges et al, *Int. Conf. SISPAD 2000* (2000), p.131.

[2] C. H. Diaz et al, *IEEE TED*, No. 6 (2001), p. 287.



(b)

Fig. 1 (a) The schematic diagram for modeling the gate line edge roughness effect using 2-D simulation tool and (b) histogram showing gate length variation in each segment following Gaussian distribution.

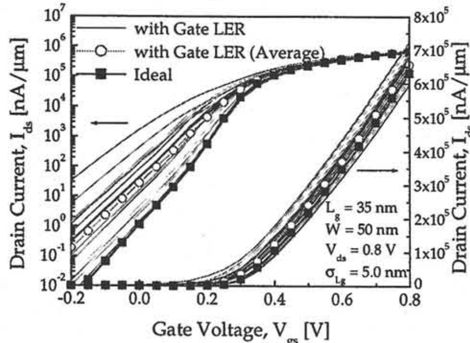


Fig. 2 I_{ds} vs. V_{gs} for 35 nm gate length MOSFET with LER σ_{Lg} = 5 nm. 30 devices with different gate line segments were calculated. It is shown that LER effect becomes very severe in 35 nm technology.

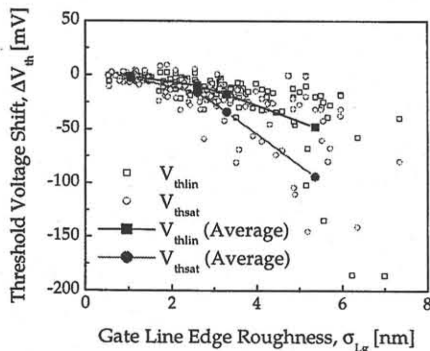


Fig. 3 Threshold voltage shift as a function of gate LER σ_{Lg} for 35 nm devices. V_{th} shift is toward the negative direction and ΔV_{thsat} is significantly degraded due to high LER.

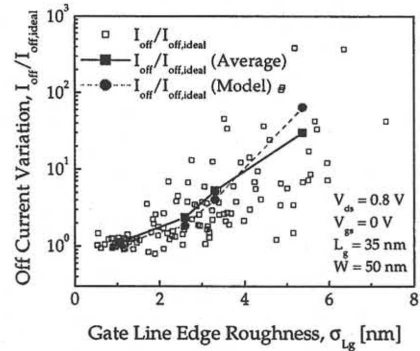


Fig. 4 Off current variation as a function of gate LER σ_{Lg} for 35 nm devices. The simplified modeling results are included. I_{off} is exponentially increased more than 10 times at $\sigma_{Lg} > 5$ nm.

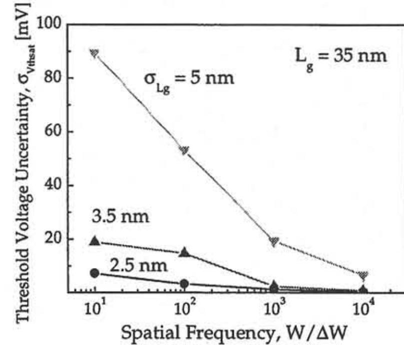


Fig. 5 Standard deviation of threshold voltage as a function of spatial frequency (W/ΔW) for 35 nm devices. The variance decreases with increasing spatial frequency.

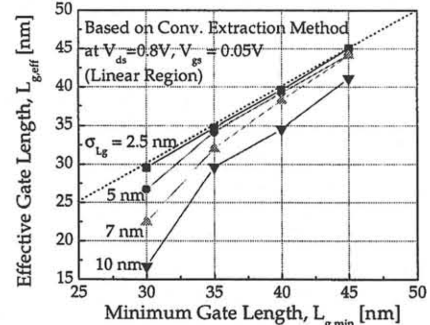


Fig. 6 LER effect on conventional effective gate length extraction method as a function of minimum gate length for 35 nm devices. The extracted electrical gate lengths are found to be shorter than real average gate lengths and much shorter as σ_{Lg} increases or $L_{g,\,min}$ decreases due to LER effect.

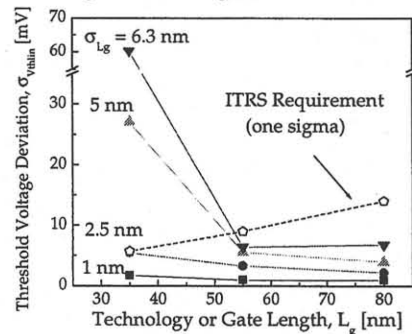


Fig. 7 Standard deviation of threshold voltage due to LER as a function of CMOS technology generation predicted by this work. To meet projection of ITRS roadmap, much more accelerated progress in lithography and gate line formation process must be challenged for reducing LER.