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Statistical Modeling of MOS Devices for Parametric Yield Prediction

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Abstract – In the manufacturing of VLSI circuits, engineering designs should take into consideration random variations arising from processing. In this paper, statistical modeling of MOS devices is reviewed, and effective and practical models are developed to predict the performance spread (i.e., parametric yield) of MOS circuits due to the process variations. To illustrate their applications, the models are applied to the 0.25 μm CMOS technology, and measured data are included in support of the model calculations.

I. Introduction

The performance of any MOS devices and integrated circuits is influenced by two different variations due to MOS processing uncertainties: interdie variation (i.e., chip to chip variation) and intradie variation (i.e., variation within the same chip, or called MOS mismatch). In digital circuits, where the outputs are dependent upon the raw value of the transistor current, the circuit performance spread is mostly effected by the interdie variation. On the other hand, the intradie variation is more important for analog circuits, where the outputs depend mostly on the ratio of transistors rather than their absolute value.

In this paper, the concept of statistical modeling is presented, and a new and practical MOS model to account for the interdie variation is developed. The model is then applied to the 0.25 μm CMOS technology to illustrate their applications in the manufacturing of MOS ICs.

II. Statistical Modeling for Interdie Variation

In our approach, a set of simulated test data is extracted first from the parametric test data using appropriate statistical analysis. Such a data has a much smaller size than the parametric test data, yet still accurately representing the MOS behavior. The simulated test data is then optimized and used to generate a set of critical parameters of a MOS model, such as BSIM3v3 [1]. Circuit simulations are then carried out to predict the circuit performance spreads.

Fig. 1 shows the flowchart of the present method (solid arrows) and conventional methods (dashed arrows). While both methods use similar statistical analysis, the main difference is that in the present approach the simulated test data (i.e., D* in flowchart) is first extracted from measurements, whereas in the conventional approach the device model (i.e., BSIM3v3) parameters (i.e., P in flowchart) are first optimized from measurements. Using the matrix size given in the flowchart, it is evident that the present approach can greatly reduce the number of optimizations needed to generate the MOS models for circuit simulation. Also, the optimized device models (i.e., P* in flowchart) resulted from the present approach can better reflect the physical behavior of the MOS devices measured.

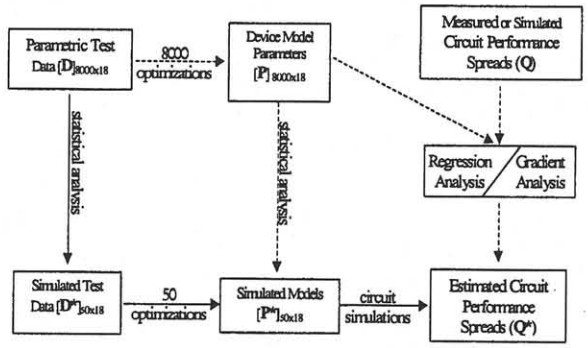

Figure 1. Flowchart for conventional (dashed arrows) and present (solid arrows) statistical modeling approaches.

The compact MOSFET model used in this study is BSIM3v3 model. A technique for selecting and extracting critical BSIM3 model parameters via optimization algorithms from the parametric test data is first discussed. Generally, the functional performances of MOSFET digital circuits are determined by three transistor characteristics: saturation current I_{ON} (the drain current when both drain voltage V_{ds} and gate voltage V_{gs} equal to supply voltage), transconductance β (defined as $\beta = gm^{max} \times 10^6/V_{ds}$, where gm^{max} is the maximum transconductance), and threshold voltage V_T. These data are typically measured on five chips per wafer. On each chip, transistors of various geometries are measured, and NMOS and PMOS transistors having the following three geometries are considered: long-channel/wide-channel, short-

channel/wide-channel, and short-channel/narrow-channel devices (see Table 1).

MOS type	Long/Wide (μm)	Short/Wide (μm)	Short/Narrow (μm)
NMOS	15/15	0.32/15	0.32/0.64
PMOS	15/15	0.28/15	0.28/0.64

Table 1. NMOS and PMOS device geometries considered for the extraction of critical BSIM3 model parameters.

The goal of the statistical model is to generate a few but statistically sufficient numbers of device models that can resemble the device statistics extracted from large sets of measurements. These device models, when implemented in circuit simulation, shall be able to predict the variance of circuit performance (i.e., parametric yield).

To improve circuit simulation efficiency, the sample of device models should be as few as possible while maintaining valid device statistics. An advanced sampling technique, Latin Hypercube Sampling (LHS) technique [2], is used in this study in order to reduce the number of simulation samples. By using the LHS, we are able to use only a few tens of samples to achieve the same effect that would require hundreds of samples using simple random sampling. The transistor models derived from this approach can then be incorporated into circuit simulation.

III. Model Applications in Digital Circuits

To illustrate the applications in circuit design, the proposed statistical model was applied to a 0.25μm CMOS process at Agere Systems, Orlando, Florida, USA and to estimate the delay time bounds of a CMOS ring oscillator circuit consisting of 501 stages of inverter. Data were collected on dies fabricated during one month from a single fabrication line. In the circuit, the size (width/length) of the NMOS is 2.66/0.32, and the size (width/length) of the PMOS is 3.66/0.28. Figure 2 shows the histogram plots of the circuit delay times measured from about 700 inverter ring oscillator circuits. Also included in the figure are the results obtained from the present and the existing worst-case models. Clearly, the present model generates more accurate lower and upper bounds than the existing model.

The delay time spread of the oscillator was also simulated using the statistical model developed with 30 sample devices, as shown in Figure 3. It is demonstrated that the statistical model is in good agreement with the measured delay time spread and gives much more quantitative and precise predictions than the worst-case analysis. Moreover, this is achieved with a minimal computation resource of only 30 sample devices.

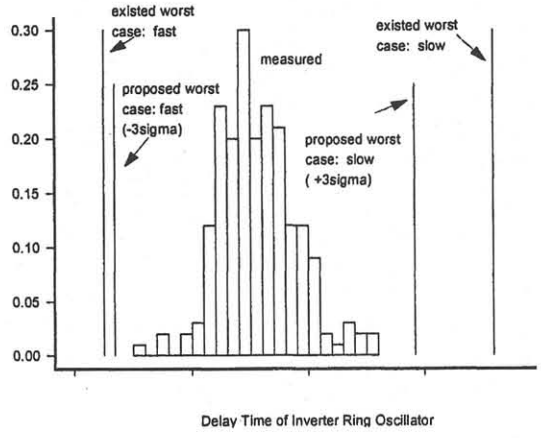

Figure 2. Measured delay time spreads, and the delay time bounds predicted by the proposed and existing worst-case analyses for a 501-stage inverter ring oscillator.

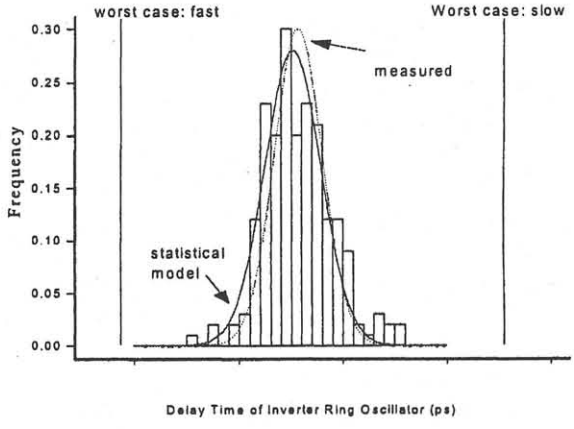

Figure 3. Measured delay time distribution (bars and the dotted line) of a 501-stage inverter ring oscillator compared with the results of the statistical simulation (solid line). The upper and lower worst-case bounds are also shown.

IV. References

[1] BSIM3v3 Users' Manual, 1999.

[2] I. C. Kizilyalli, T. E. Ham, K. Singhal, J. W. Kearney, W. Lin, and M. J. Thoma, "Predictive worst case statistical modeling of 0.8-μm BICMOS bipolar transistor: a methodology based on process and mixed device/circuit level simulation," IEEE Trans. Electron Devices, Vol. 40, no.5, pp. 966-973, 1993.